ROM 3

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
Read Only Memories			
5K ROM	5,120 bits organized 512 x 10	RO-3-5120	3-4
16K ROM	16,384 bits organized 2,048 x 8	RO-3-8316A	3-6
		RO-3-8316B	3-6
		RO-3-9316A	3-6
		RO-3-9316B	3-6
		RO-3-9316C	3-6
32K ROM	32,768 bits organized 4,096 x 8	RO-3-9332A	3-11
		RO-3-9332B	3-11
64K ROM	65,536 bits organized 8,192 x 8	RO-3-9364B	3-14
Keyboard Encoders			
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	AY-5-2376	3-18
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	AY-5-3600	3-23
		AY-5-3600-PRO	3-29
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	AY-3-4592	3-32
Character Generator			
CHARACTER GENERATOR	2,560 bits organized as 64 - 5 x 8 characters.	RO-3-2513	3-44

GENERAL INSTRUMENT

Read Only Memories

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
5K ROM	5,120 bits organized 512 x 10	RO-3-5120	3-4
16K ROM	16,384 bits organized 2,048 x 8	RO-3-8316A	3-6
		RO-3-8316B	3-6
		RO-3-9316A	3-6
		RO-3-9316B	3-6
		RO-3-9316C	3-6
32K ROM	32,768 bits organized 4,096 x 8	RO-3-9332A	3-11
		RO-3-9332B	3-11
64K ROM	65,536 bits organized 8,192 x 8	RO-3-9364B	3-14

5120 Bit Static Read Only Memory

FEATURES

- 512×10 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns Maximum Access Time
- 150mW Typical Power
- Three-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

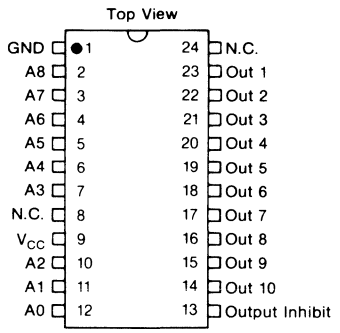
DESCRIPTION

The General Instrument RO-3-5120 is a 5120 bit static Read-Only-Memory. It is organized as 512 ten bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-5120 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

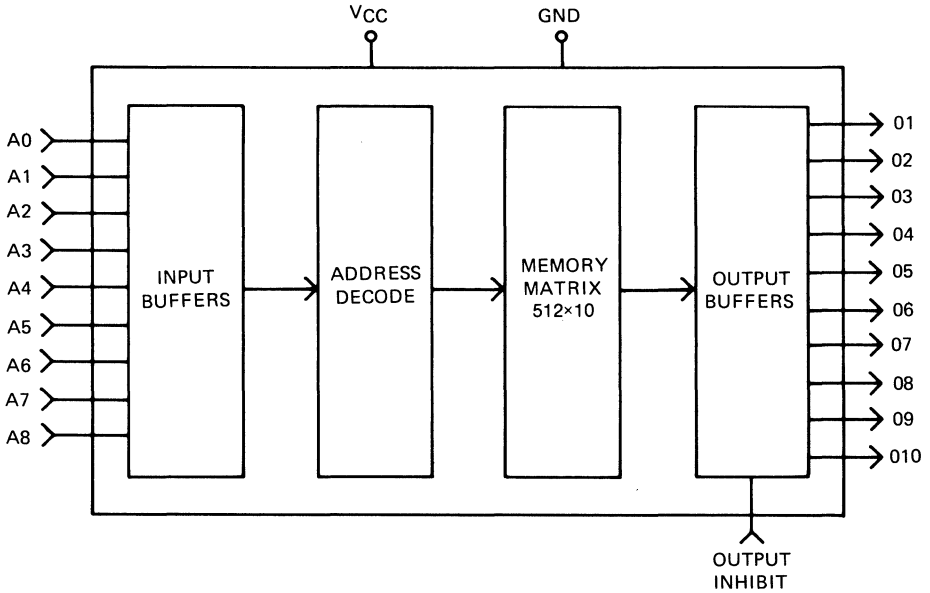
A separate publication, "RO-3-5120 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-5120 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

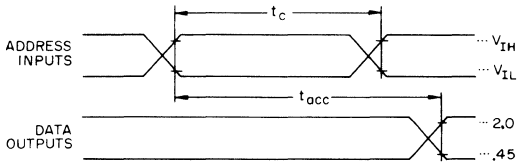
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 50pF

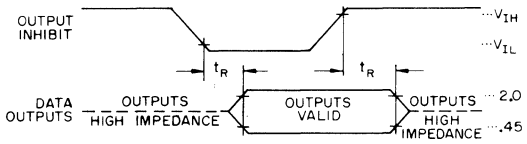
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	30	45	mA	Outputs Open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	230	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

ROM

16384 Bit Static Read Only Memories

FEATURES

- 2048 x 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 850ns Maximum Access Time: RO-3-8316A/9316A
- 450ns Maximum Access Time: RO-3-8316B/9316B
- 350ns Maximum Access Time: RO-3-9316C
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The General Instrument RO-3-8316A/8316B and RO-3-9316A/9316B/9316C are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-8316A/8316B and RO-3-9316A/9136B/9316C offer the best combination of high performance, large bit storage, and simple interfacing.

The RO-3-8316A/8316B are direct replacements in pin connection and operation for the Intel 8316A and 2316A.

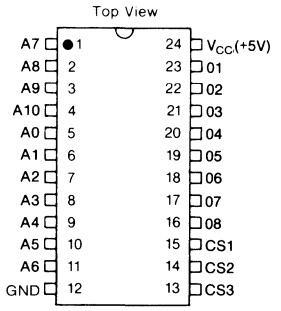
The RO-3-9316A/9316B/9316C pin configuration is identical to that of the Intel 2716 16K EPROM.

A separate publication, "RO-3-8316/9316 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming.

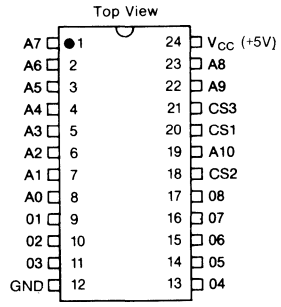
PIN CONFIGURATION

24 LEAD DUAL IN LINE

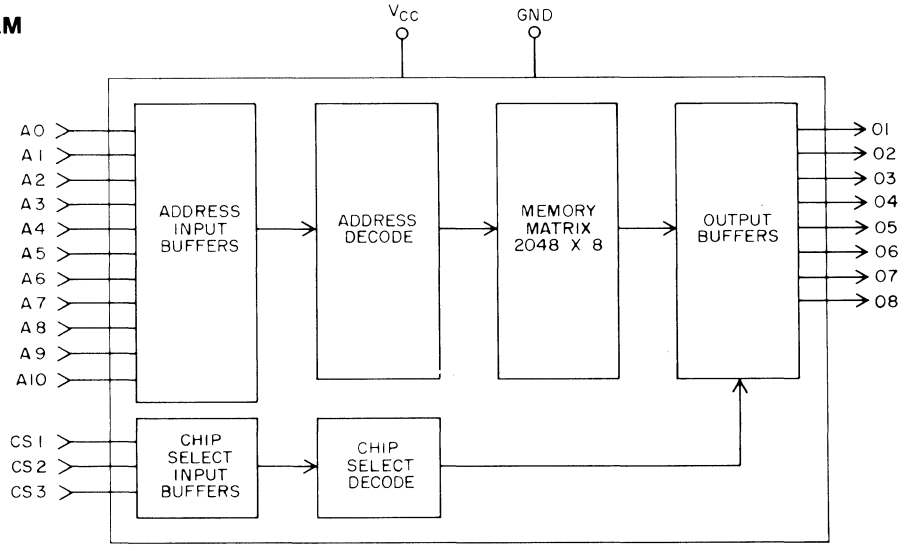
RO-3-8316A/8316B



RO-3-9316A/9316B/9316C



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 100pF.

RO-3-8316A/9316A, RO-3-8316B/9316B, and RO-3-9316C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-8316A/9316A	I_{CC}	—	50	85	mA	Outputs open
RO-3-8316B/9316B	I_{CC}	—	65	95	mA	Outputs open
RO-3-9316C	I_{CC}	—	—	105	mA	Outputs open

RO-3-8316A/9316A

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-8316B/9316B

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-9316C

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

**Typical values are at +25°C and nominal voltages.

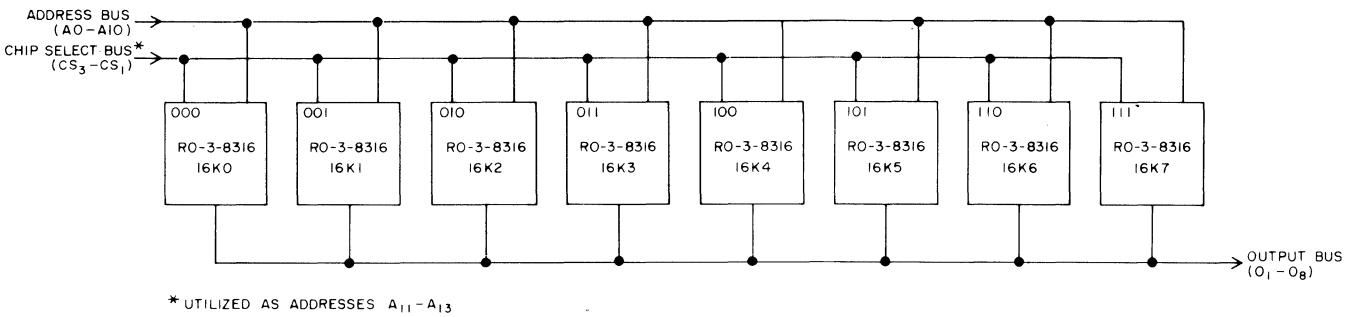
ROM

TYPICAL SYSTEM APPLICATION

A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programmable chip select features and by wiring the outputs of eight different RO-3-8316's as shown in the figure below.

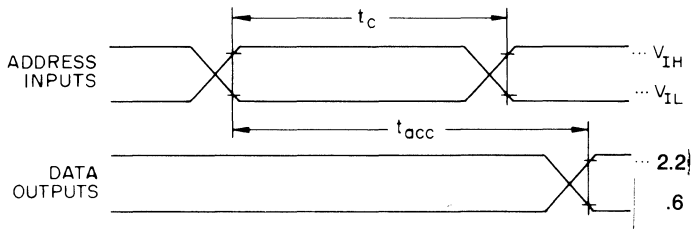
CHIP SELECT TABLE

CS3	CS2	CS1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7

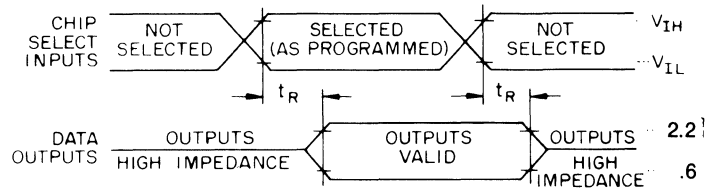


*UTILIZED AS ADDRESSES A_{11}-A_{13}

TIMING DIAGRAMS

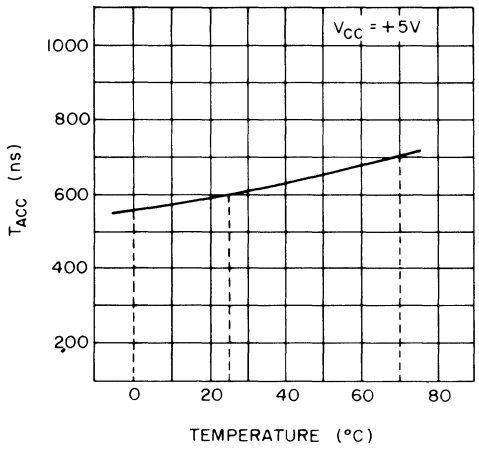


ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)

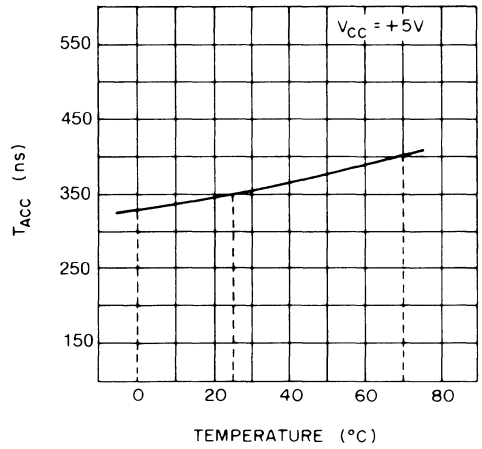


CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

TYPICAL CHARACTERISTIC CURVES

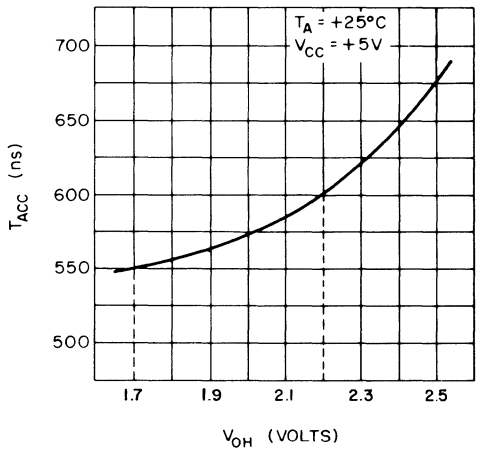


RO-3-8316A/9316A

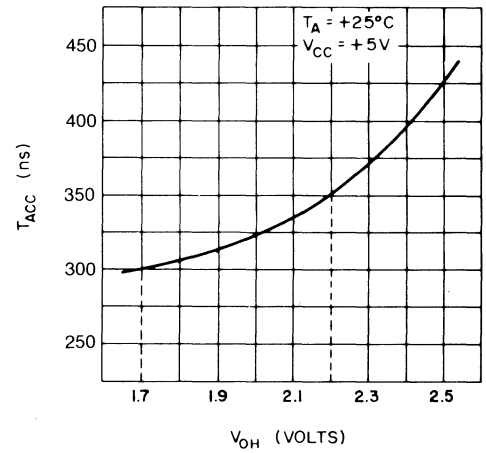


RO-3-8316B/9316B

Fig.1 ACCESS TIME VS. TEMPERATURE

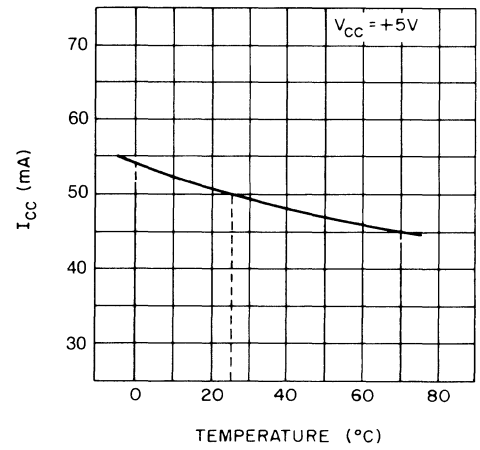


RO-3-8316A/9316A

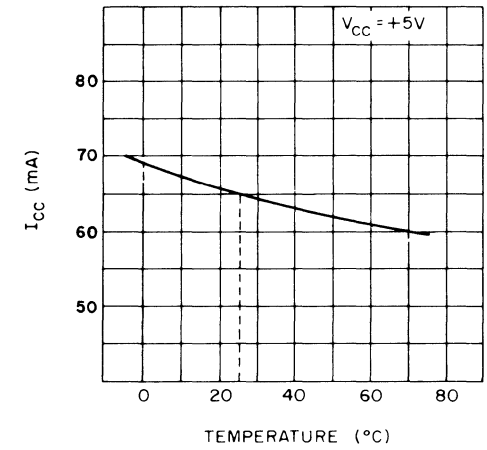


RO-3-8316B/9316B

Fig.2 ACCESS TIME VS. OUTPUT VOLTAGE



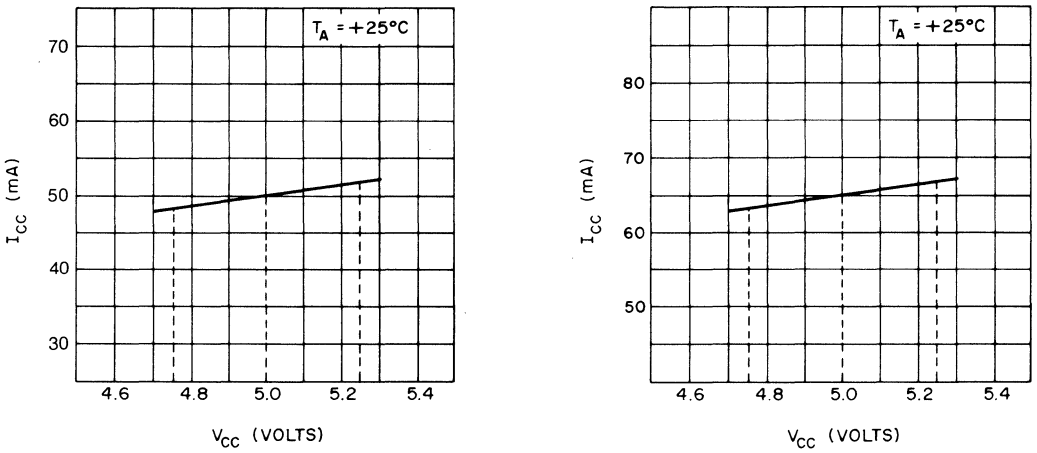
RO-3-8316A/9316A



RO-3-8316B/9316B

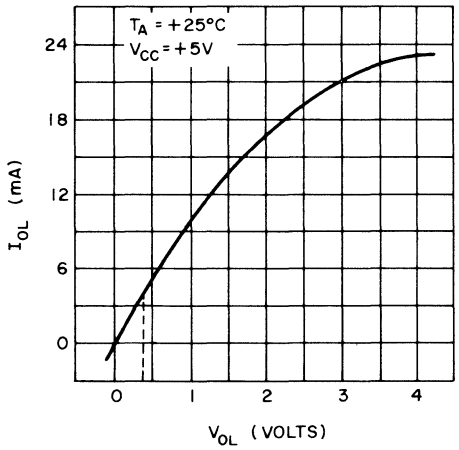
Fig.3 POWER SUPPLY CURRENT VS. TEMPERATURE

TYPICAL CHARACTERISTIC CURVES



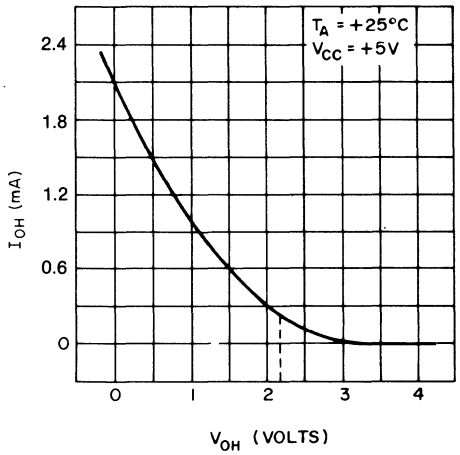
RO-3-8316A/9316A **RO-3-8316B/9316B**

Fig.4 POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.5 OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.6 OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

32768 Bit Static Read Only Memory

FEATURES

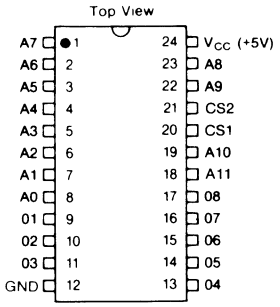
- 4096 × 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 850ns Maximum Access Time: RO-3-9332A
- 450ns Maximum Access Time: RO-3-9332B
- Three-State Outputs—under the control of two mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

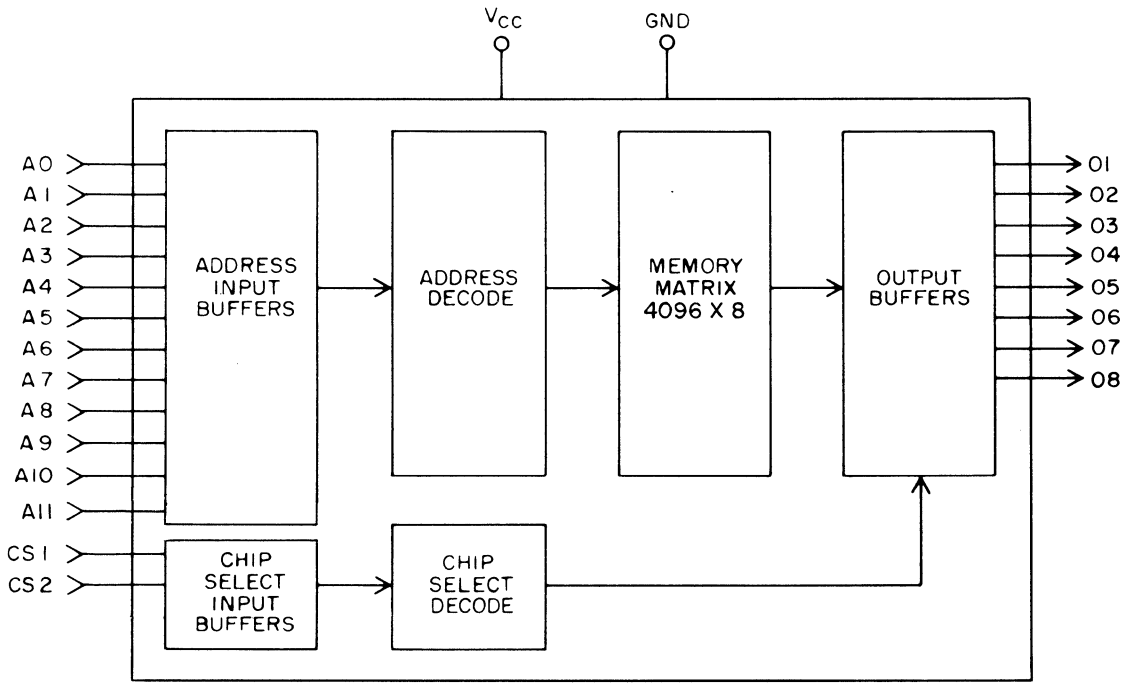
The General Instrument RO-3-9332A/9332B are 32,768 bit static Read Only Memories organized as 4096 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advance GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9332A/9332B offer the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±10%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pF

RO-3-9332A/9332B

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9332A	I_{CC}	—	—	60	mA	Outputs open
RO-3-9332B	I_{CC}	—	—	125	mA	Outputs open
RO-3-9332C	I_{CC}	—	—	140	mA	Outputs open

RO-3-9332A

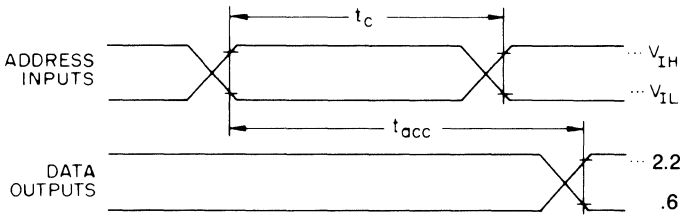
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-9332B

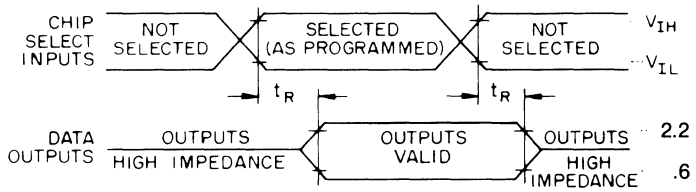
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	450	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

ROM

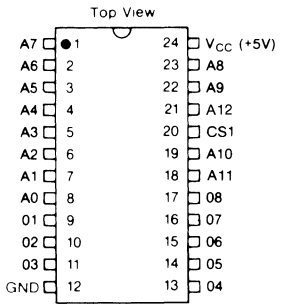
65536 Bit Static Read Only Memory

FEATURES

- 8192 x 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Edge-activated
- 450ns Maximum Access Time
- Three-State Outputs
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

PIN CONFIGURATION

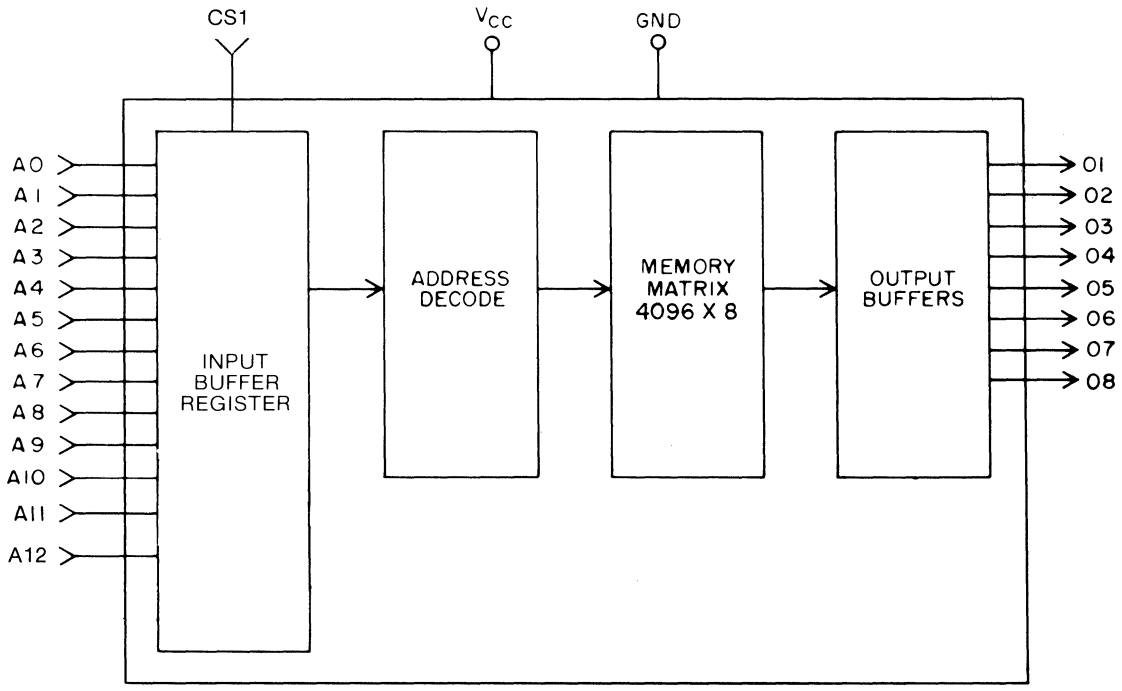
24 LEAD DUAL IN LINE



DESCRIPTION

The General Instrument RO-3-9364B is a 65,536 bit static Read Only Memory organized as 8192 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9364B offers the best combination of high performance, large bit storage, and simple interfacing.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) ..... −0.5V +7.0V
Storage Temperature ..... −65°C to +150°C
Operating Temperature (T_A) ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

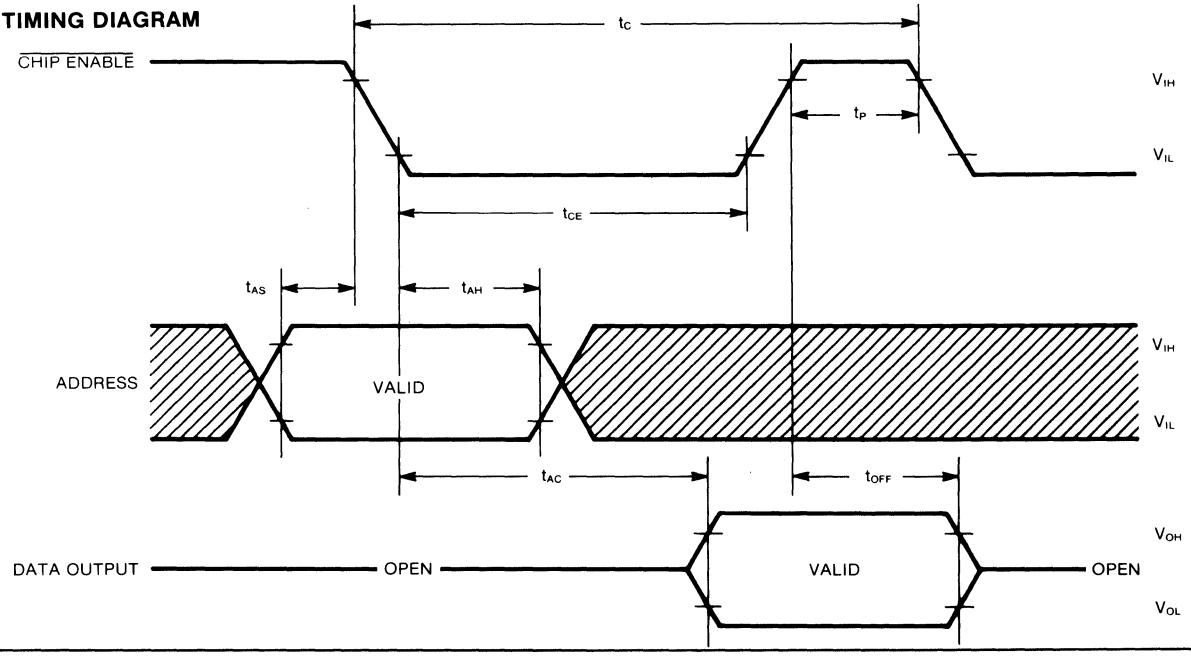
Standard Conditions (unless otherwise noted)

V_{CC}=+5 Volts ±10%
Operating Temperature (T_A)=0°C to +70°C
Output Loading: two TTL Loads, $C_{L\ TOTAL}$=100pF

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, $\overline{\text{Chip Enable}}$ Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH}=200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL}=3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC} (Active)	—	—	—	50	mA	Output Loading=1MΩ and 100pF $\overline{\text{CE}}$ at Minimum Cycle Time
I_{CC} (Standby)	—	—	—	10	mA	$\overline{\text{CE}}$=Logic "1"
AC CHARACTERISTICS						
Cycle Time	t_C	400	—	—	ns	All outputs Driving two TTL Loads and 100pF
$\overline{\text{CE}}$ Pulse Width	t_{CE}	300	—	—	ns	
$\overline{\text{CE}}$ Precharge Time	t_P	100	—	—	ns	
$\overline{\text{CE}}$ Access Time	t_{AC}	—	—	300	ns	
Output Turn Off Time	t_{OFF}	—	—	75	ns	
Address Set Up Time	t_{AS}	0	—	—	ns	
Address Hold Time	t_{AH}	75	—	—	ns	
CAPACITANCE						
Input Capacitance	C_I	—	—	7	pF	f=1MHz
Output Capacitance	C_O	—	—	10	pF	f=1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



Keyboard Encoders

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	AY-5-2376	3-18
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	AY-5-3600	3-23
		AY-5-3600-PRO	3-29
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	AY-3-4592	3-32

ROM

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- External control provided for output polarity selection
- External control provided for selection of odd or even parity
- Two key roll-over operation
- N-key lockout
- Programmable coding with a single mask change
- Self-contained oscillator circuit
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

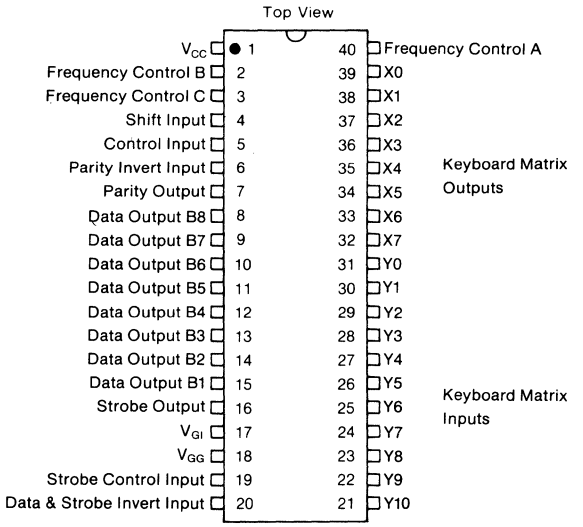
DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

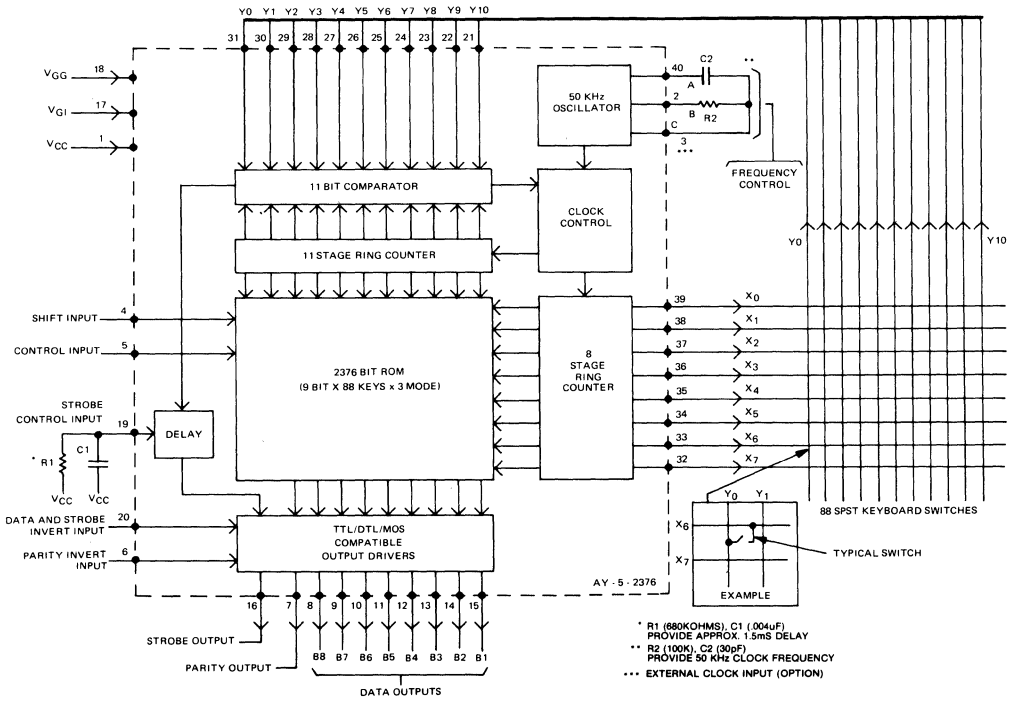
The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram) a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

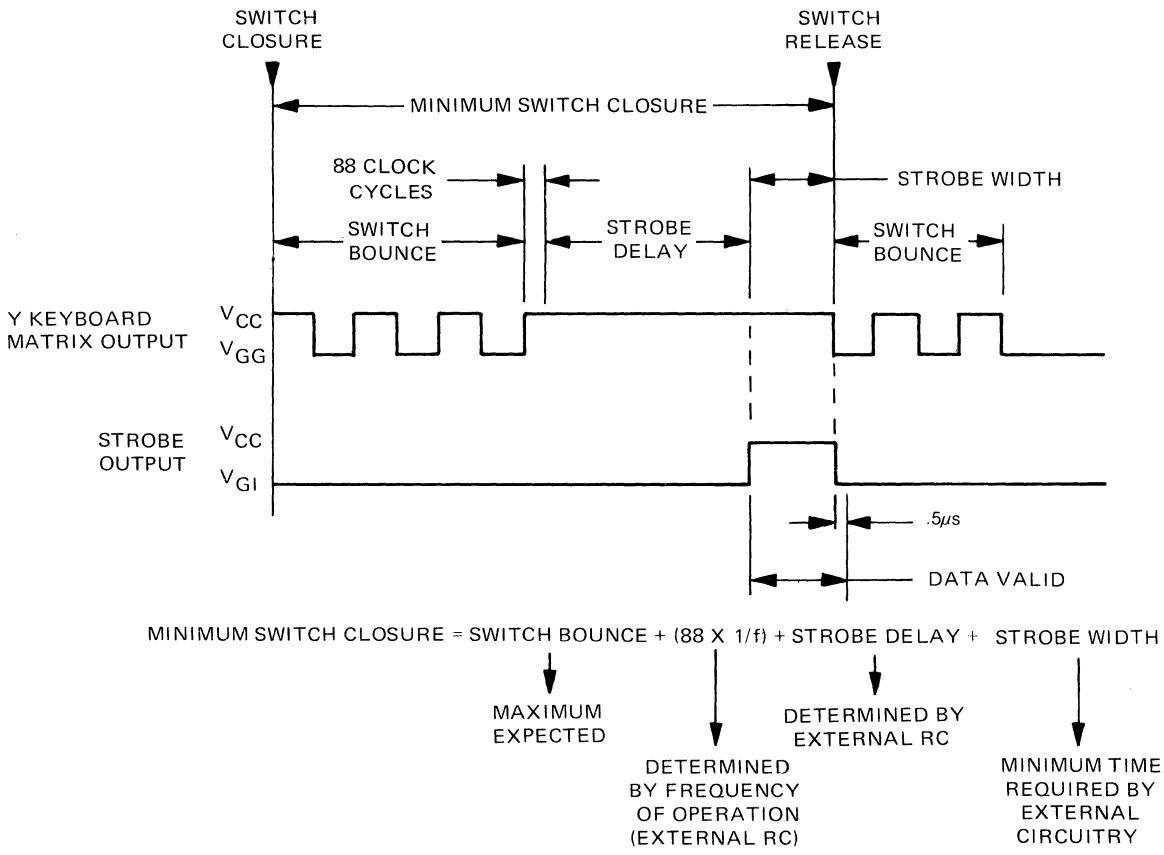
The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and 9, the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

ROM

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

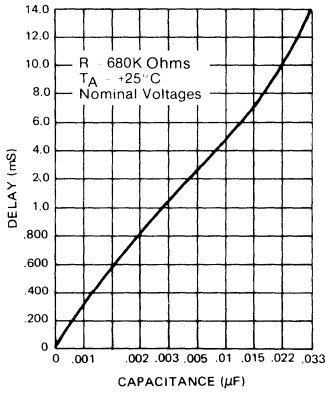
V_{CC} = +5 Volts ± 0.5 Volts, (V_{CC} = Substrate Voltage)
V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{XI}	—	0	—	μA	$V_{OUT} = V_{CC}$
		80	150	400	μA	$V_{OUT} = V_{CC}$ −1.3V
		140	300	800	μA	$V_{OUT} = V_{CC}$ −2.0V
		250	700	1500	μA	$V_{OUT} = V_{CC}$ −5V
		500	1500	3000	μA	$V_{OUT} = V_{CC}$ — 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	$V_{OUT} = V_{CC}$
		13	27	65	μA	$V_{OUT} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{OUT} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{OUT} = V_{CC}$ −5V
		—	1	20	μA	$V_{OUT} = V_{CC}$ −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	$V_{IN} = V_{CC}$
		26	54	130	μA	$V_{IN} = V_{CC}$ −1.3V
		24	50	120	μA	$V_{IN} = V_{CC}$ −2.0V
		10	20	80	μA	$V_{IN} = V_{CC}$ −5V
		—	2	20	μA	$V_{IN} = V_{CC}$ −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	$V_{IN} = V_{CC}$
		13	27	65	μA	$V_{IN} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{IN} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{IN} = V_{CC}$ −10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680K to V_{SS}
Data Output (B_1-B_9)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

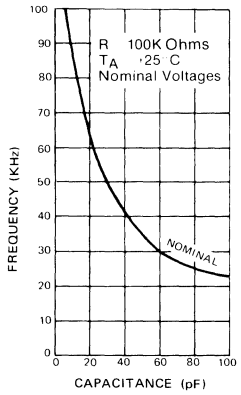
**Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

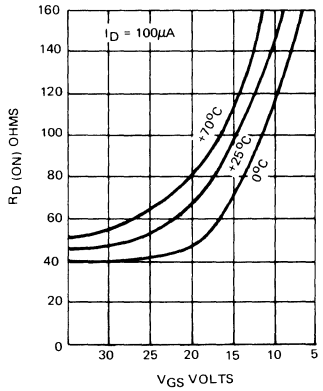
TYPICAL CHARACTERISTIC CURVES



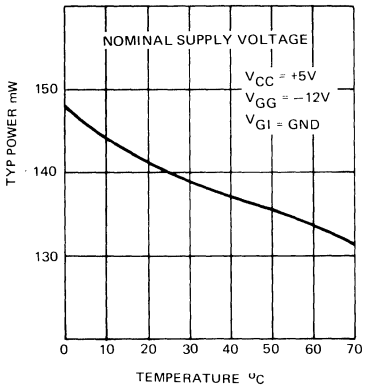
STROBE DELAY C1



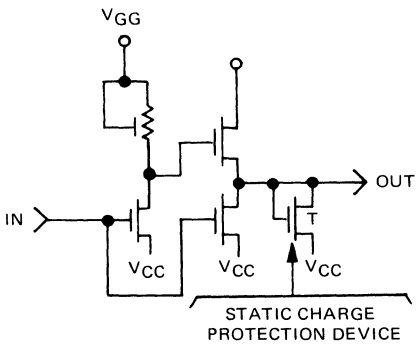
OSCILLATOR FREQUENCY VS. C2



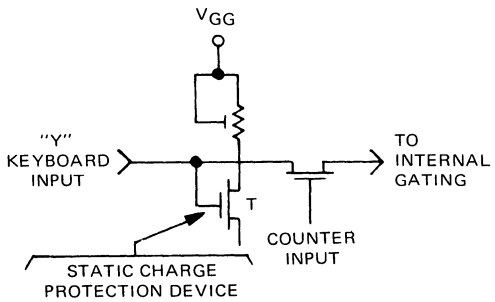
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



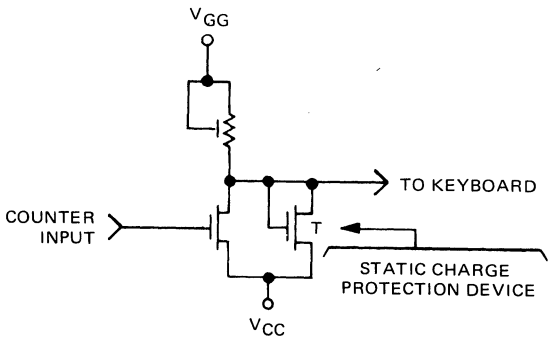
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (°C)



OUTPUT DRIVER

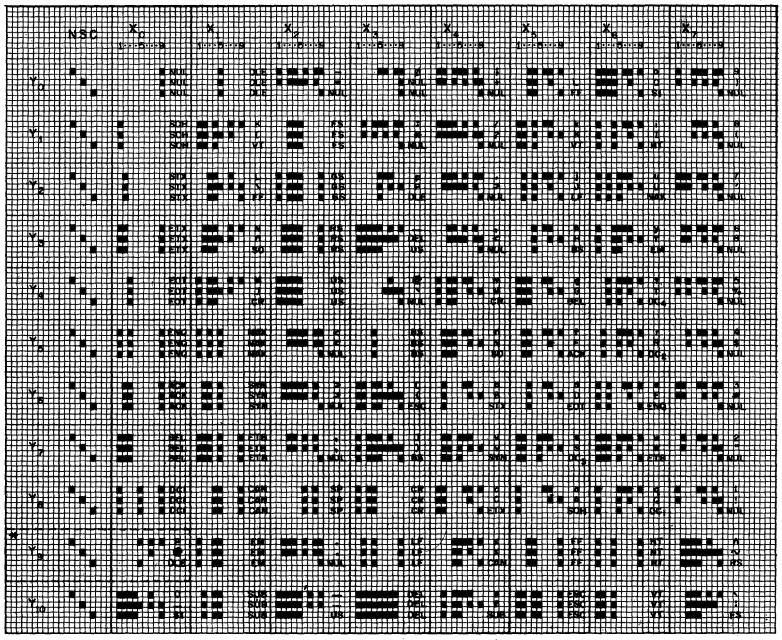


"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

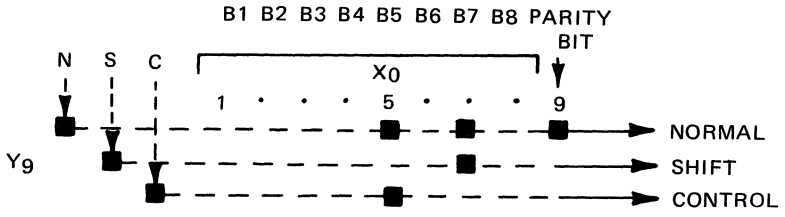
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

*EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0 — Y_9 AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}\ \overline{C}$ = N
$\underline{S}\ \overline{C}$ = S
$\overline{S}$ C = C
S C = C

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit
- 10 output data bits available
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Output data buffer register included
- Output enable provided (option)
- External data complement control provided (option)
- Pulse or level data ready output signal provided (option)
- "Any Key Down" output provided (option)
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Programmable coding with a single mask change
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

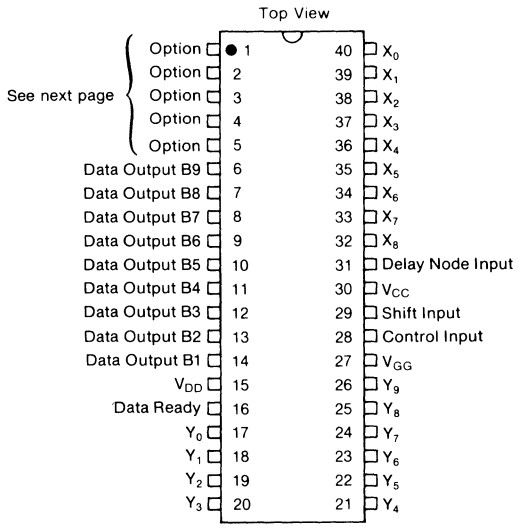
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

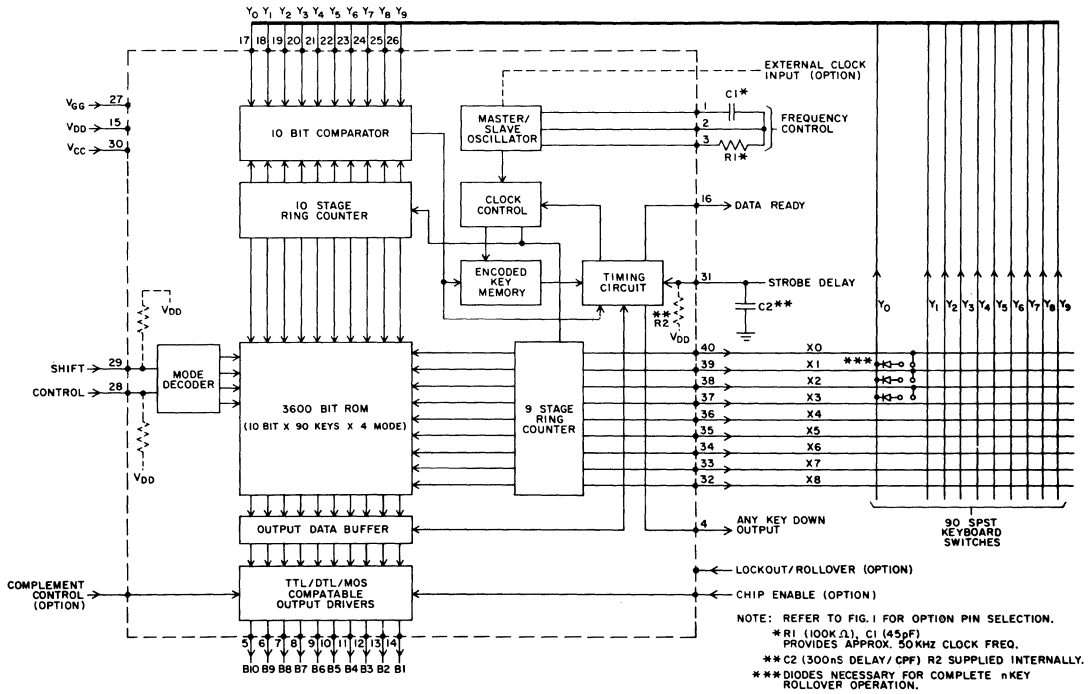
The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package pin to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC})	−20V to +0.3V
Logic input voltages (with respect to V_{CC})	−20V to +0.3V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A) = 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Clock Input	V_{I0}	V_{GG}	—	.15	V	
	V_{I1}	V_{CC} −1.4	—	V_{CC} +0.3	V	
Data Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.75	V	
Logic "1" Level	V_{I1}	V_{CC} −1.1	—	V_{CC}+0.3	V	
Shift & Control Input Current	I_{NSC}	75	95	120	μA	V_I = +5V
X Output (X_0-X_8)						
Logic "1" Output Current	I_{XI}	40	170	400	μA	V_{OUT} = V_{CC} (See Note 2)
		600	1300	2500	μA	V_{OUT} = V_{CC}−1.3V
		900	1600	3500	μA	V_{OUT} = V_{CC}−2.0V
		1500	3800	6000	μA	V_{OUT} = V_{CC}−5V
		3000	6000	10000	μA	V_{OUT} = V_{CC}−10V
Logic "0" Output Current	1_{XO}	8	15	50	μA	V_{OUT} = V_{CC}
		6	11	35	μA	V_{OUT} = V_{CC}−1.3V
		5	10	30	μA	V_{OUT} = V_{CC}−2.0V
		2	5	15	μA	V_{OUT} = V_{CC}−5V
		—	0.5	5	μA	V_{OUT} = V_{CC}−10V
Y Input (Y_0-Y_9)						
Trip Level	V_Y	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	V_{IN} = V_{CC}
		14	28	90	μA	V_{IN} = V_{CC}−1.3V
		13	25	80	μA	V_{IN} = V_{CC}−2.0V
		6	12	60	μA	V_{IN} = V_{CC}−5V
		—	1	30	μA	V_{IN} = V_{CC}−10V
Unselected Y Input Current	I_{YU}	9	18	50	μA	V_{IN} = V_{CC}
		7	14	45	μA	V_{IN} = V_{CC}−1.3V
		6	13	40	μA	V_{IN} = V_{CC}−2.0V
		3	6	30	μA	V_{IN} = V_{CC}−5V
		—	0.5	15	μA	V_{IN} = V_{CC}−10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	φP	1500	3500	5000	μA	V = V_{CC}
		200	600	1500	μA	V = V_{CC}−5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	.55	V	I_{OL} = .25mA
	—	—	—	0.8	V	I_{OL} = 1.6mA
Logic "1"	—	V_{CC} −1.3	—	—	V	I_{OH} = .95mA
Power						
I_{CC}	—	—	8	13	mA	V_{CC} = +5V
I_{GG}	—	—	8	13	mA	V_{GG} = −12V

**Typical values are at +25°C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

ROM

OPERATION

The AY-5-3600 contains (see Block Diagram) a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

ROM

TIMING DIAGRAM

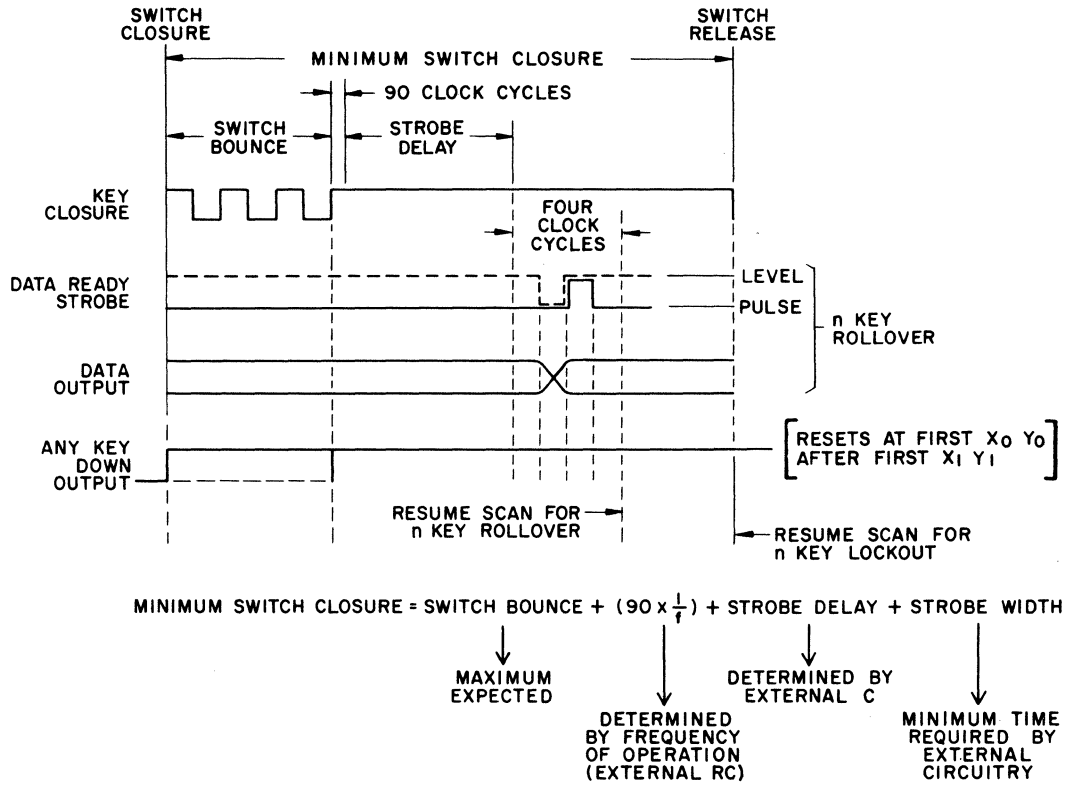


Fig.1

SYMBOL	MODE N	S	C	SC
@		X1 Y0, X0 Y8		
A		X0 Y2		X1 Y2
B		X5 Y3		X2 Y2
C		X2 Y3		X3 Y2
D		X2 Y2		X4 Y2
E		X2 Y1		X5 Y2
F		X3 Y2		X6 Y2
G		X4 Y2		X7 Y2
H	X0 Y5	X0 Y5, X5 Y2	X0 Y5	X0 Y5
I		X7 Y1		X0 Y4
J		X6 Y2		X6 Y6
K		X7 Y2		X3 Y6
L	X2 Y6	X2 Y6, X8 Y2	X2 Y6	X2 Y6
M		X7 Y3		X3 Y5
N		X6 Y3		X4 Y5
O		X8 Y1		
P		X6 Y6		X0 Y2, X0 Y3
Q		X0 Y1		X1 Y3
R		X3 Y1		X2 Y3
S		X1 Y2		X4 Y3
T		X4 Y1		X5 Y3
U		X0 Y1		X6 Y3
V		X4 Y3		X7 Y3
W		X1 Y1		X6 Y5
X		X1 Y3		X8 Y2
Y		X5 Y1		X5 Y6
Z		X0 Y3		X5 Y5
a	X0 Y2		X0 Y2	
b	X5 Y3		X5 Y3	
c	X2 Y3		X2 Y3	
d	X2 Y2		X2 Y2	
e	X2 Y1		X2 Y1	
f	X3 Y2		X3 Y2	
g	X4 Y2		X4 Y2	
h	X5 Y2		X5 Y2	
i	X7 Y1		X7 Y1	
j	X6 Y2		X6 Y2	
k	X7 Y2, X2 Y9		X7 Y2	
l	X8 Y2		X8 Y2	
m	X7 Y3, X1 Y6		X7 Y3	
n	X6 Y3, X1 Y8		X6 Y3	
o	X8 Y1		X8 Y1	
p	X6 Y6, X0 Y8		X6 Y6	
q	X0 Y1		X0 Y1	
r	X3 Y1		X3 Y1	
s	X1 Y2		X1 Y2	
t	X4 Y1		X4 Y1	
u	X6 Y1		X6 Y1	
v	X4 Y3		X4 Y3	
w	X1 Y1		X1 Y1	
x	X1 Y3		X1 Y3	
y	X5 Y1		X5 Y1	
z	X0 Y3		X0 Y3	
[		X8 Y6, X2 Y9		X4 Y6, X8 Y6
\				X1 Y1
]	X8 Y6	X1 Y6	X8 Y6	X8 Y1
^		X1 Y8		X2 Y4
_	X4 Y7, X8 Y7		X4 Y7, X8 Y7	X4 Y7
`	X3 Y6	X3 Y6	X3 Y6	
{	X4 Y5	X4 Y5	X4 Y5	
~				X6 Y4
DEL			X2 Y9	X2 Y9
NULL	X5 Y7	X5 Y7	X5 Y7, X0 Y8	X5 Y7, X0 Y8

SYMBOL	MODE N	S	C	SC
SOH			X0 Y9	X5 Y0, X0 Y9
STX			X1 Y9	X4 Y0, X1 Y9
ETX	X4 Y4	X4 Y4	X4 Y4	X4 Y4, X6 Y0
EOT				X4 Y1
ENQ				X3 Y1
ACK			X2 Y8	X7 Y1, X2 Y8
BEL			X3 Y8	X6 Y1, X3 Y8
BS				X3 Y4
HT	X0 Y4	X0 Y4	X0 Y4, X8 Y9	X8 Y9
LF	X7 Y6	X7 Y6	X7 Y6	
VT	X3 Y7	X3 Y7	X3 Y7	X3 Y7
FF	X7 Y8		X7 Y8	X7 Y8
CR	X3 Y5	X3 Y5	X3 Y5, X1 Y6	X1 Y6
SO	X0 Y7		X0 Y7, X1 Y8	X0 Y7, X1 Y8
SI	X1 Y7	X1 Y7	X1 Y7	X1 Y7
DLE				X0 Y1
DC1				X5 Y1
DC2				X6 Y7
DC3				X2 Y1
DC4				X3 Y0
NAK				X2 Y0
SYN				X5 Y4
ETB				X1 Y0
CAN	X3 Y4		X3 Y4	
EM				X8 Y0
SUB				X0 Y0
ESC				X7 Y0
FS				X1 Y4
GS				X7 Y6
RS	X1 Y4	X1 Y4	X1 Y4	
US	X2 Y7	X2 Y7	X2 Y7	X2 Y7
SP	X3 Y3, X4 Y9	X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y3
!	X5 Y9	X5 Y9, X0 Y9	X5 Y9	X5 Y9
"	X3 Y9	X3 Y9, X7 Y5, X1 Y9	X3 Y9	X3 Y9, X7 Y5
#	X6 Y9	X6 Y9, X2 Y0	X6 Y9	X6 Y9
$	X2 Y5	X2 Y5, X3 Y0	X2 Y5	X2 Y5
%	X1 Y5	X1 Y5, X4 Y0	X1 Y5	X1 Y5
&	X6 Y8	X6 Y0, X6 Y8, X2 Y8	X6 Y8	X6 Y8
'	X7 Y5	X3 Y8	X7 Y5	X7 Y4
(	X7 Y9	X7 Y4, X3 Y4, X8 Y0	X7 Y9	X7 Y9
)	X4 Y8	X4 Y8, X6 Y7, X8 Y9	X4 Y8	X4 Y8
*	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	X5 Y8
+	X0 Y6	X0 Y6, X5 Y6, X7 Y7	X0 Y6	X0 Y6, X7 Y7
,	X8 Y3	X8 Y3	X8 Y3	X8 Y3
-	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X8 Y7
.	X8 Y4	X8 Y4	X8 Y4	X8 Y4
/	X7 Y4		X7 Y4	
0	X6 Y7, X8 Y8	X8 Y8	X6 Y7, X8 Y8	X8 Y8
1	X0 Y0, X0 Y9		X0 Y0	
2	X1 Y0, X1 Y9		X1 Y0	
3	X2 Y6		X2 Y0	
4	X3 Y0		X3 Y0	
5	X4 Y0		X4 Y0	
6	X5 Y0, X2 Y8		X5 Y0	
7	X6 Y0, X3 Y8		X0 Y0	
8	X7 Y0		X7 Y0	
9	X8 Y0, X8 Y9		X8 Y0	
:	X5 Y4	X8 Y5	X5 Y4	X8 Y5
;	X8 Y5, X5 Y6		X8 Y5, X5 Y6	
<	X6 Y5	X7 Y8, X6 Y5, X0 Y0	X6 Y5	
=	X6 Y4, X7 Y7	X7 Y7, X6 Y4, X4 Y7	X6 Y4	
>	X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	
?	X4 Y6	X4 Y6, X7 Y4	X4 Y6	

Note 1. Bits 1 to 6 and bit 8 of the AY-5-3600 correspond to bits 1 to 7 of ASC II.

Note 2. Codes 0000011 and 0011111 are not present in the standard AY-5-3600 pattern.

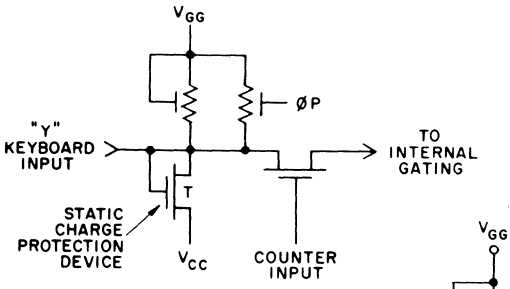
Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS ASCII CODE

OPTIONS PROVIDED WITH STANDARD ENCODER

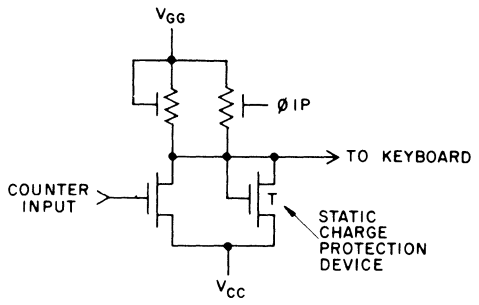
- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3
- Any Key Output on Pin No. 4
- Any Key Output True (Logic 1) During Key Depression
- Output Data Bit B10 on Pin No. 5
- N-Key Rollover Only
- True Outputs Only
- Pulse Data Ready Signal
- Internal Resistor to V_{DD} on Shift/Control Pin
- Plastic Package

ROM

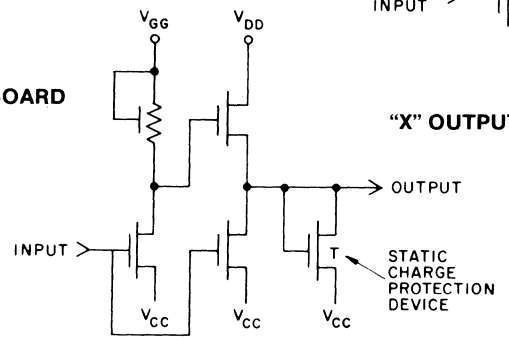
Fig.3



"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD



OUTPUT DRIVER

NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}.

TYPICAL CHARACTERISTIC CURVES

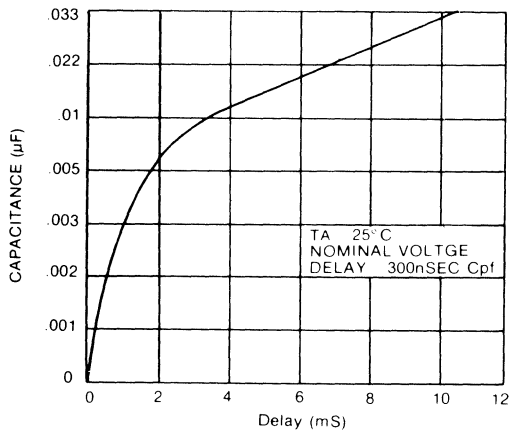


Fig.4 STROBE DELAY vs. C_1

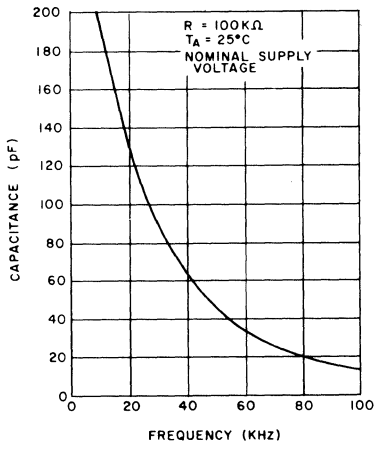


Fig.5 OSCILLATOR FREQUENCY vs. C_2

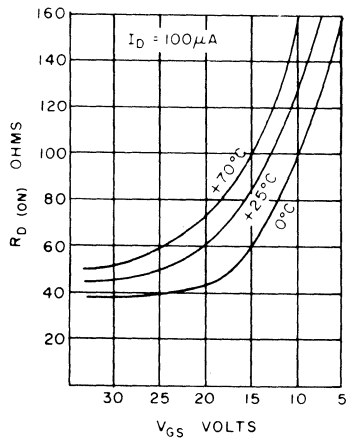


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

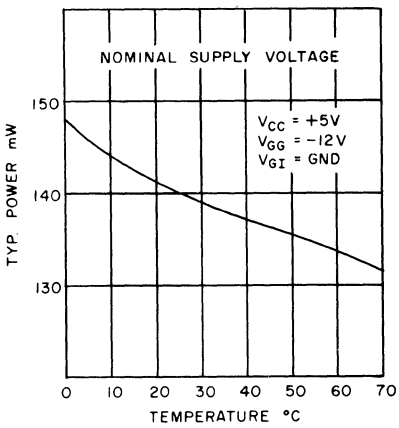
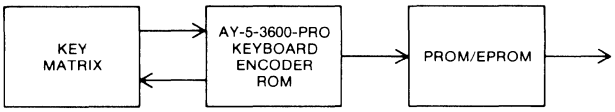


Fig.7 TYPICAL POWER CONSUMPTION (mW)

Keyboard Encoder and PROM/EPROM Application

The AY-5-3600-PRO is pre-programmed during manufacture to provide specific yet simple binary coded outputs thus allowing the purchase of off-the-shelf devices (distributors, etc.). To enhance the device flexibility, the binary outputs have been organized to provide direct interface with a PROM/EPROM.



The PROM (Programmable Read Only Memory) permits the programming of the required output code in the factory or the field within minutes, thus making it extremely suitable for small quantity, fast turnaround keyboard requirements. The EPROM (Erasable Programmable Read Only Memory) is ideally suited for prototyping, where patterns are quite variable, allowing the EPROM to be erased and reprogrammed repeatedly. Similar advantages are realized in the field where pattern changes are necessary in order to respond to redefined requirements or to subtle system peculiarities not previously encountered.

Technical Description

The AY-5-3600-PRO is a binary coded MOS-LSI device programmed to furnish 360 unique 9-bit codes (90 keys × 4 modes × 9 bits). Option selections include such popular functions as Internal Oscillator, Lockout/Rollover and an Any Key Down output. For further, more explicit device characteristics refer to the preceding pages. The internal oscillator is a self contained (on-chip) circuit option which eliminates the need for any external clock source. For applications necessitating an external clock source the internal oscillator input pins may be utilized to function in the slave mode of operation. Lockout or Rollover is selectable via an input pin, thus allowing the versatility required on various keyboard applications. The Any Key Down output performs the function of a gating signal by acknowledging both a key depression and release, making it a convenient signal for use in a repeat application.

For ease of translation, each key is assigned an X-Y coordinate and, in turn, each X-Y coordinate has been identified with a specific yet simple binary coded output. Two formats are described: the first for application with a 64 key 4 mode keyboard and the second for a 90 key 4 mode keyboard.

The 64 key 4 mode application as illustrated in Fig. 8 utilized keyboard encoder addresses X0 Y0 thru X6 Y3. A unique combination of one input (Y) and one output (X) is assigned to each key, for a total coverage of 64 keys. Binary coded outputs B2-B9 have been arranged to provide the necessary 8-bit address inputs to the PROM/EPROM, with B2 and B3 representing the variable mode identification and B4-B9 each specific key closure.

When a key is depressed a path is completed between one X line and one Y line thus addressing that specific X-Y ROM coordinate in the AY-5-3600-PRO. The 8-bit binary code for that X-Y location (ref. Truth Table page 14-15) is transferred into a one character 8-bit output latch (B2-B9) thus providing the appropriate 8-bit address to the 256 x 8 PROM/EPROM.

Expansion to a 90 key 4 mode operation (see Fig. 9) is identical to the 64 key 4 mode except: the 90 key 4 mode version utilizes the full complement of addresses X0 Y0 thru X8 Y9 (90 keys). The 8-bit binary code (B2-B9) previously produced to address the 256 x 8 PROM/EPROM is now expanded to a 9-bit binary code (B1-B9) for addressing to a 512 x 8 PROM/EPROM. With expansion to a 90 key 4 mode application outputs B1-B3 now serve as the variable mode identification.

The interface to a PROM/EPROM enables the custom programming of the required output data in the PROM/EPROM to directly coincide to the specific address inputs from the AY-5-3600-PRO. Any PROM whether it be bipolar, ultraviolet erasable or electrically alterable, may be employed to provide a wide variety of "off-the-shelf" keyboards. Once the keyboard assembly has gone beyond the prototyping stage, and assuming the quantity/cost permit, the PROM/EPROM data can be converted to the standard AY-5-3600 data format (ref. AY-5-3600 Custom Coding Information sheet) and produced in production quantities. This eliminates the PROM/EPROM expense while assuring the absence of undefined coding changes.

Summary of Important Features

- Ability to deliver complete keyboard assemblies within days without sacrificing the features offered in the AY-5-3600 Keyboard Encoder
- Ability to buy off-the-shelf devices (distributor, etc.)
- Ability to verify the specific pattern format using a PROM/EPROM prior to a 'custom' encoder commitment

NORMAL

X	Y	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	2	0	0	0	0	0	0	0	1	0
0	3	0	0	0	0	0	0	0	1	1
0	4	0	0	0	0	0	0	1	0	0
6	3	0	0	0	1	1	1	1	1	1

6 OF 8 Bit ADDRESS

MODE IDENT. ILLUSTRATED USING NORMAL MODE ONLY, FOR REMAINING MODES REFER TO TRUTH TABLE

64 x 4 BLOCK DIAGRAM

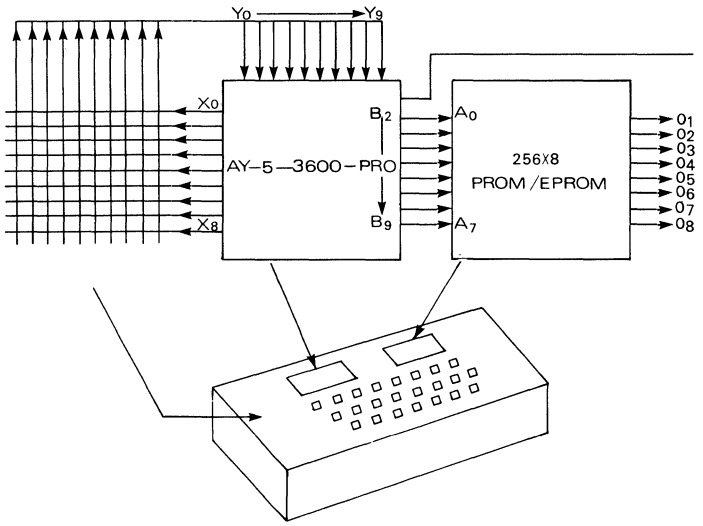


Fig.8 64 KEY 4 MODE KEYBOARD APPLICATION

NORMAL

X	Y	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	2	0	0	0	0	0	0	0	1	0
0	3	0	0	0	0	0	0	0	1	1
0	4	0	0	0	0	0	0	1	0	0
8	9	1	0	0	0	1	1	0	0	1

6 OF 9 Bit ADDRESS

MODE IDENT. ILLUSTRATED USING NORMAL MODE ONLY, FOR REMAINING MODES REFER TO TRUTH TABLE

90 x 4 BLOCK DIAGRAM

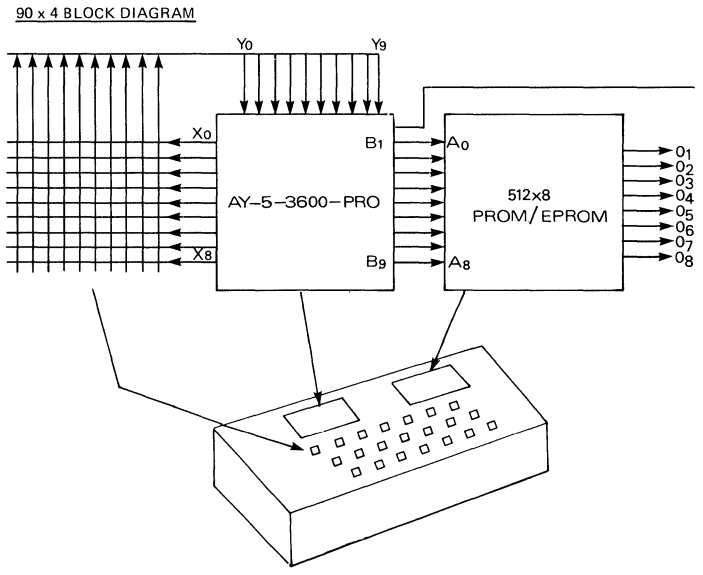


Fig.9 90 KEY 4 MODE KEYBOARD APPLICATION

OPTIONS

- Device Marking: AY-5-3600-PRO
- Internal Oscillator on Pin Nos. 1, 2, 3
- Lockout/Rollover on Pin No. 4
  Internal Resistor to V_{DD} on Lockout/Rollover Pin
- True Outputs Only
- Any Key Output on Pin No. 5.
  Any Key Output True (Logic 1) During Key Depression
- Pulse Data Ready Signal
- Plastic Package
- Internal Resistor to V_{DD} on Shift/Control Pin

XY	NORMAL	SHIFT	CONTROL	SHFT/CTR	XY	NORMAL	SHIFT	CONTROL	SHFT/CTR
0	000000000	001000000	010000000	011000000	45	000101101	001101101	010101101	011101101
1	000000001	001000001	010000001	011000001	46	000101110	001101110	010101110	011101110
2	000000010	001000010	010000010	011000010	47	000101111	001101111	010101111	011101111
3	000000011	001000011	010000011	011000011	48	000110000	001110000	010110000	011110000
4	000000100	001000100	010000100	011000100	49	000110001	001110001	010110001	011110001
5	000000101	001000101	010000101	011000101	50	000110010	001110010	010110010	011110010
6	000000110	001000110	010000110	011000110	51	000110011	001110011	010110011	011110011
7	000000111	001000111	010000111	011000111	52	000110100	001110100	010110100	011110100
8	000001000	001001000	010001000	011001000	53	000110101	001110101	010110101	011110101
9	000001001	001001001	010001001	011001001	54	000110110	001110110	010110110	011110110
10	000001010	001001010	010001010	011001010	55	000110111	001110111	010110111	011110111
11	000001011	001001011	010001011	011001011	56	000111000	001111000	010111000	011111000
12	000001100	001001100	010001100	011001100	57	000111001	001111001	010111001	011111001
13	000001101	001001101	010001101	011001101	58	000111010	001111010	010111010	011111010
14	000001110	001001110	010001110	011001110	59	000111011	001111011	010111011	011111011
15	000001111	001001111	010001111	011001111	60	000111100	001111100	010111100	011111100
16	000010000	001010000	010010000	011010000	61	000111101	001111101	010111101	011111101
17	000010001	001010001	010010001	011010001	62	000111110	001111110	010111110	011111110
18	000010010	001010010	010010010	011010010	63	000111111	001111111	010111111	011111111
19	000010011	001010011	010010011	011010011	64	100000000	101000000	110000000	111000000
20	000010100	001010100	010010100	011010100	65	100000001	101000001	110000001	111000001
21	000010101	001010101	010010101	011010101	66	100000010	101000010	110000010	111000010
22	000010110	001010110	010010110	011010110	67	100000011	101000011	110000011	111000011
23	000010111	001010111	010010111	011010111	68	100000100	101000100	110000100	111000100
24	000011000	001011000	010011000	011011000	69	100000101	101000101	110000101	111000101
25	000011001	001011001	010011001	011011001	70	100000110	101000110	110000110	111000110
26	000011010	001011010	010011010	011011010	71	100000111	101000111	110000111	111000111
27	000011011	001011011	010011011	011011011	72	100001000	101001000	110001000	111001000
28	000011100	001011100	010011100	011011100	73	100001001	101001001	110001001	111001001
29	000011101	001011101	010011101	011011101	74	100001010	101001010	110001010	111001010
30	000011110	001011110	010011110	011011110	75	100001011	101001011	110001011	111001011
31	000011111	001011111	010011111	011011111	76	100001100	101001100	110001100	111001100
32	000100000	001100000	010100000	011100000	77	100001101	101001101	110001101	111001101
33	000100001	001100001	010100001	011100001	78	100001110	101001110	110001110	111001110
34	000100010	001100010	010100010	011100010	79	100001111	101001111	110001111	111001111
35	000100011	001100011	010100011	011100011	80	100010000	101010000	110010000	111010000
36	000100100	001100100	010100100	011100100	81	100010001	101010001	110010001	111010001
37	000100101	001100101	010100101	011100101	82	100010010	101010010	110010010	111010010
38	000100110	001100110	010100110	011100110	83	100010011	101010011	110010011	111010011
39	000100111	001100111	010100111	011100111	84	100010100	101010100	110010100	111010100
40	000101000	001101000	010101000	011101000	85	100010101	101010101	110010101	111010101
41	000101001	001101001	010101001	011101001	86	100010110	101010110	110010110	111010110
42	000101010	001101010	010101010	011101010	87	100010111	101010111	110010111	111010111
43	000101011	001101011	010101011	011101011	88	100011000	101011000	110011000	111011000
44	000101100	001101100	010101100	011101100	89	100011001	101011001	110011001	111011001

ROM

Capacitive Keyboard Encoder

FEATURES

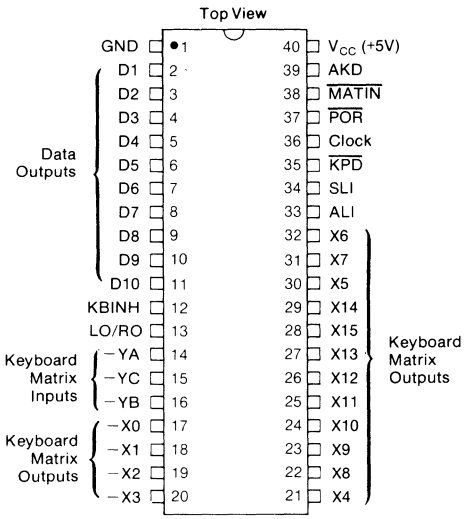
- 128 key keyboard encoder: 112 fully decoded keys, 16 discrete function keys
- 112 keys with 4 modes, 10 bit output
- Key validation logic protects against bounce
- N-key roll over or 2-key roll over
- Internal ROM allows any keys to control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK
- ALPHA LOCK and SHIFT LOCK indicator lines
- Any key down (AKD) strobe
- Single +5 Volt power supply
- Programmable coding of standard and special function keys
- Zener diode protection on all I/O pins
- Low power consumption, less than 2 milliwatts per key
- Usable with capacitive, magnetic, inductive. Hall effect or mechanical keyboard switches
- Inputs and outputs TTL and CMOS compatible
- Internal Oscillator

DESCRIPTION

The G.I. AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programmable discrete function keys. ROM programming permits any keys to control the shift control and lock functions. The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

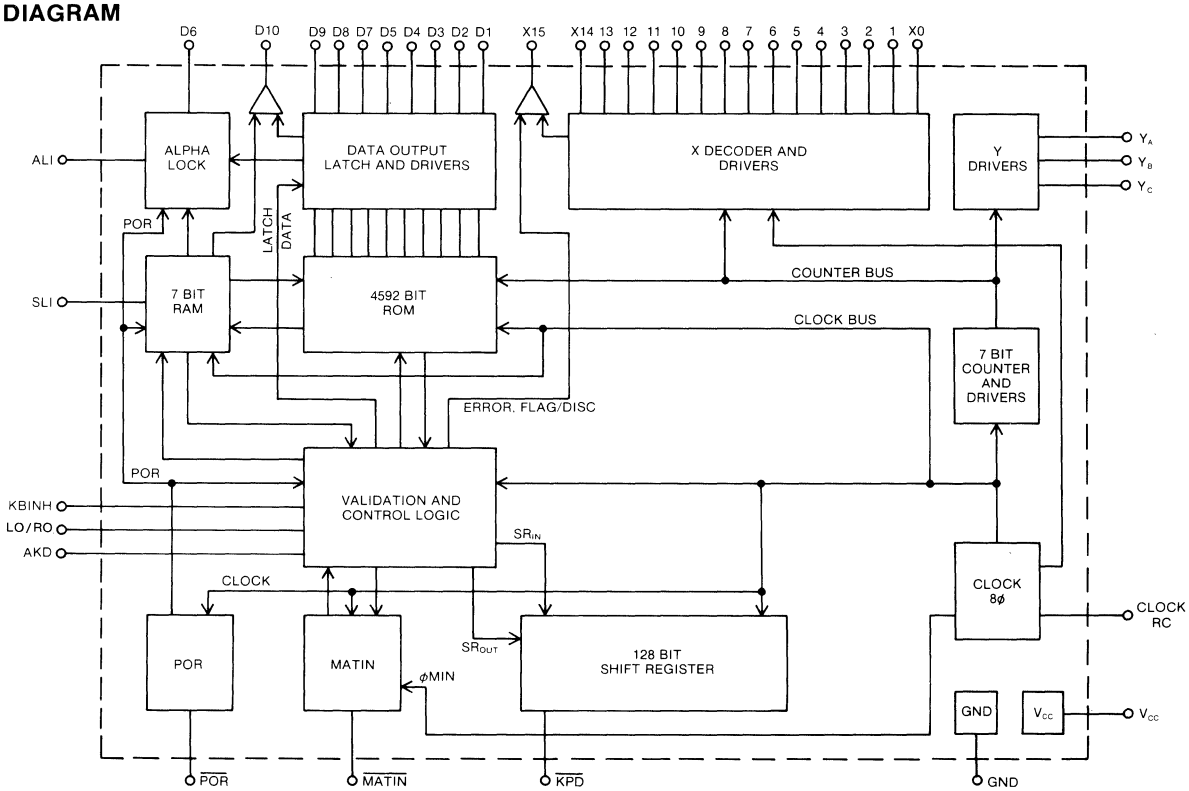
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with N-channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	Ground	GND	Ground Pin
2-10	Data Out	D1-D9	Data Outputs, D1 through D9
11	Data Out	D10	Data Output D10. See "AY-3-4592 options" for complete description
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See "AY-3-4592 options" for other custom options
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V_{CC}. This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.
28, 29	X15, 14	X15, X14	X15 is programmed as a "discrete output" key in the standard part. Optionally it may be programmed as a error flag or as a Matrix drive line. See "AY-3-4592 options". Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.
33	Alpha Lock Indicator	ALI	ALI will indicate if "op code" XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.
34	Shift Lock Indicator	SLI	SLI will indicate if "op code" XX011 is selected. (See "operation codes"). In the standard device this op code will also select the shift lock function.
35	Key Pressed	$\overline{KPD}$	$\overline{KPD}$ is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition $\overline{KPD}$ may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected $\overline{KPD}$ is generated causing the 8 bit latch output to go high. See figure 2.
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:
37	Reset	$\overline{POR}$	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.
38	Matrix Input	$\overline{MATIN}$	Input from external multiplexer. Senses signal from X-Y scan of depressed key.
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depresed AKD goes high. If while one key is held, a second key is depressed AKD will go low for 2 clock cycles.
40	Power	V_{CC}	Power supply input; +5 Volts

	C = 150pf		C = 220pf		C = 500pf	
R	Freq	Scan time	Freq	Scan time	Freq	Scan time
5K	1.3 MHz	1.5 msec	1.2 MHz	1.7 msec	.71 MHz	2.8 msec
10K	.8 MHz	2.3 msec	.8 MHz	2.7 msec	.45 MHz	4.3 msec
25K	.4 MHz	4.8 msec	.3 MHz	6.0 msec	.20 MHz	10.0 msec

ROM

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 msec, at a 1.2MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse width, 90ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programming of the AY-3-4592, keys may have one of three different functions. Keys on matrix lines X0 through X13 have in addition to the output code bits a function flag bit (FFB). If the FFB is programmed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the "op code" and are used to provide special functions such as shift, shift lock, alpha lock etc. Bits 6-10 are not used.

Op codes may be programmed to provide data outputs as well as change the mode of operation. Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programmed as one indicates a "down-coded" key, for which the 10 data bits programmed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programmed as one indicates an "up-coded" key for which the 10 data bits programmed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 nor 5 will have any effect on the operational control of bits 10-3.

Table 1

Op-Code 5	4	3	2	1	Function
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	X15 may be programmed as 1) an X-output to provide a second set of 8 discrete lines 2) a "discrete output" which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See "Error Flag" In the AY-3-4592 STD X15 is a discrete output
Error Flag	When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programmed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the "automatic reset" is selected/the flag will be reset when the error causing Key is released. Op-code XX110 may be programmed on a function key to reset the error flag. If pin 12 is programmed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles. In the AY-3-4592 STD, error flag causes KBINH and is automatically reset.
Alpha Lock	When programmed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33). When Alpha lock is not programmed, op code XX101 will simply result in an output on ALI (pin 33). Op code XX101 may be programmed for momentary action, or latched push-on, push-off alternating action. ALI may be programmed for normally low or high output. Op code XX101 is momentary action. ALI is normally low. The AY-3-4592 STD is not programmed for Alpha lock, although there will be an output on ALI.
Shift Lock	When programmed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34). If shift lock is not programmed, op code XX011 will simply cause an output on SLI. SLI may be programmed for normally low or high output. The AY-3-4592 STD is programmed for shift lock operation with SLI normally low.
KBINH	KBINH, Keyboard Inhibit, may be programmed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programmed, as a group, to be inhibited by KBINH. This is the "KCI Out" option. When pin 12 is programmed to cause KBINH, a "high" input on pin 12 will inhibit processing of common keys. If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released. The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The "KCI In" option is used, that is, the function key operation is independent of KBINH.
D10	D10, pin 11, may be programmed as the output for the memory bit 10 or as a "discrete" output. As a discrete output pin 10 is switched from its normal state (programmable as high or low) by the function key with op-code XX111. The AY-3-4592 STD is programmed for D10 as a discrete key, normally low.
Key Type	Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... -0.3 Volts to +7.0 Volts
Maximum voltage with respect to V_{CC} ..... +0.3 Volts
Storage Temperature ..... 65°C to +150°C
Operating Temperature ..... 0 to 70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

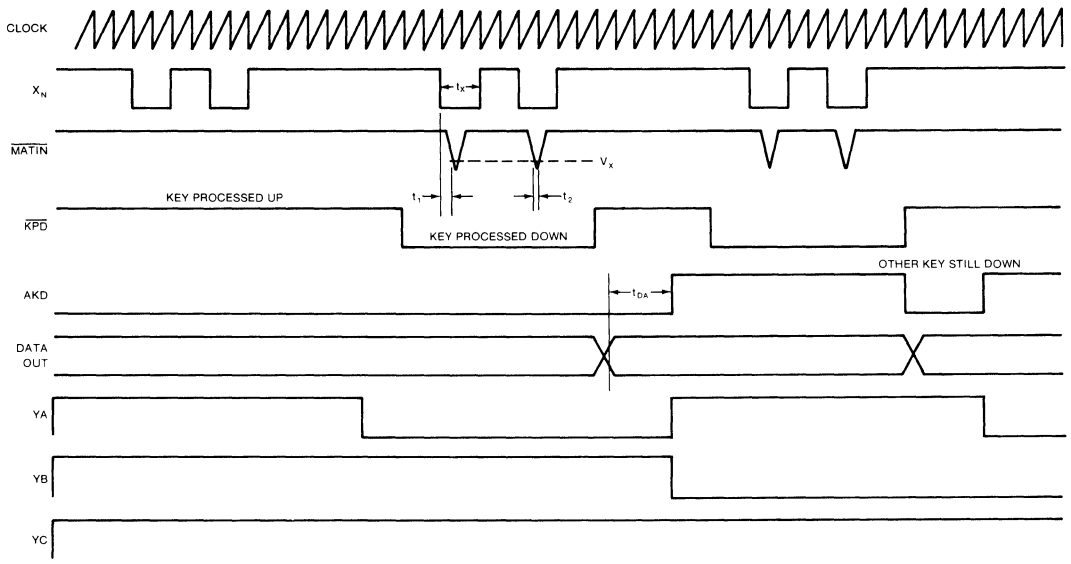
Standard Conditions (unless otherwise noted)

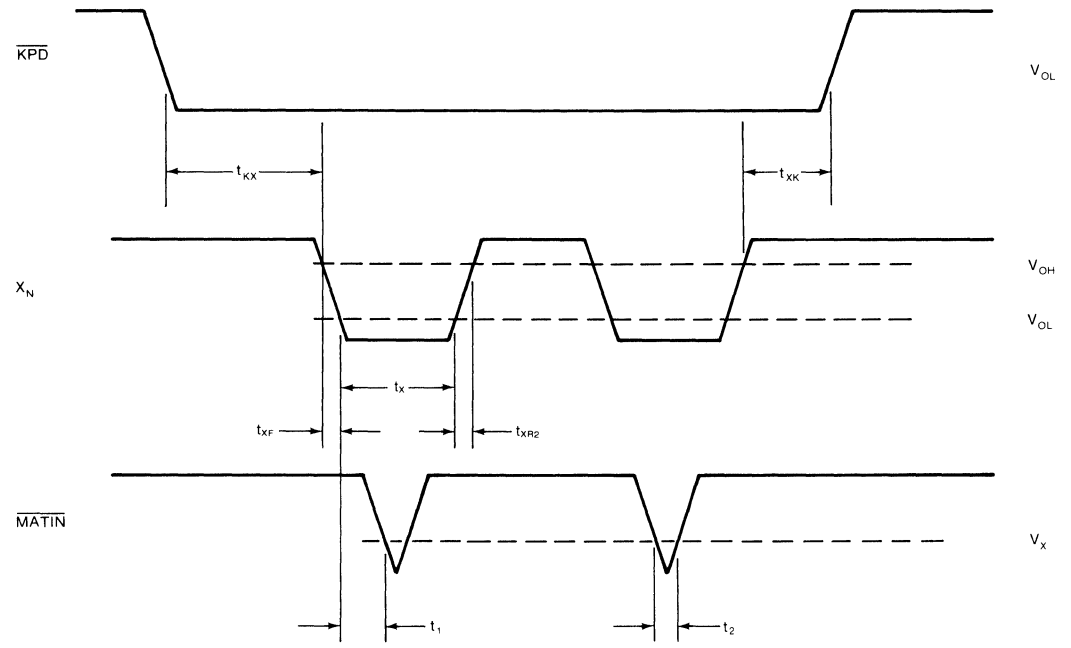
V_{CC} = 5.0V ±5%
T_A = 0° to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	I_{OH} = 50μA, 25pF
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except $\overline{POR}$, 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except $\overline{POR}$, 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	V_{in} = 5V
X Output "1" Voltage	X_{OH}	3.5	-	-	V	I_{OH} = 50μA, 100pF
X Output "0" Voltage	X_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
AKd Output Voltage	V_A	-	-	0.6	V	I_{OL} = 3.2mA
$\overline{MATIN}$ Input Voltage	V_X	-	-	0.4	V	
$\overline{POR}$, 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
$\overline{POR}$, 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	V_{CC} = 5.3V
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
X Output rise time	t_{XR1}	-	-	150	ns	V_{OH} = 2.4V, V_{OL} = 0.4V
X Output rise time	t_{XR2}	-	-	500	ns	V_{OH} = 3.5V, V_{OL} = 0.4V
X Output rise time	t_{XR3}	-	-	1500	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
$\overline{KPD}$-X Output set time	T_{KX}	500	-	-	ns	
X Output-$\overline{KPD}$ hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

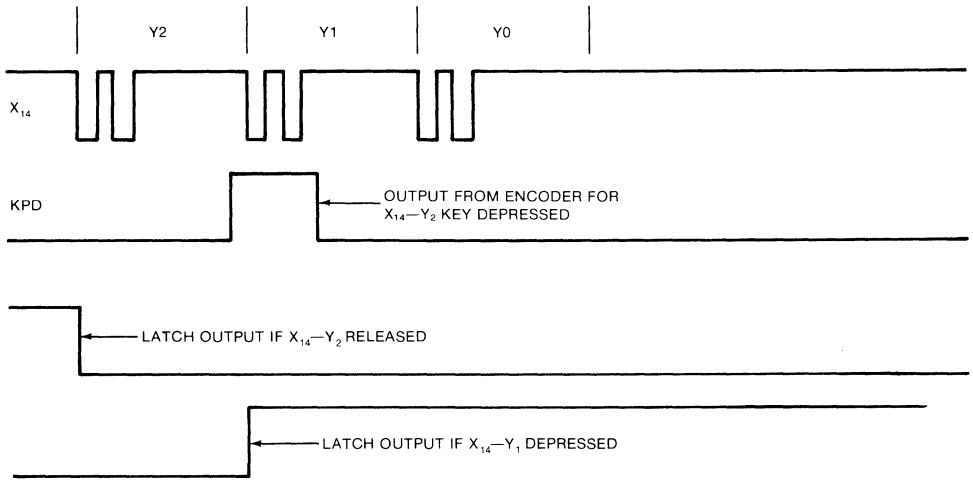
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





Discrete Function Key



CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
000	1	001	0000000001	Right Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
001	1	002	0000000010	Left Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
002	1	003	0000000011	Shift Lock	3FF	1111111111		3FF	1111111111		3FF	1111111111	
003	1	004	0000000100	Control	3FF	1111111111		3FF	1111111111		3FF	1111111111	
004	1	005	0000000101	ALI	3FF	1111111111		3FF	1111111111		3FF	1111111111	
005	1	006	0000000110	X15	3FF	1111111111		3FF	1111111111		3FF	1111111111	
006	1	007	0000000111	D10	3FF	1111111111		3FF	1111111111		3FF	1111111111	
007	0	0CE	0011001110	1	0DE	0011011110	!	0CE	0011001110	I	0DE	0011011110	I
010	0	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ES
011	0	0CD	0011001101	2	1BF	0110111111	@	0CD	0011001101	2	1FF	0111111111	NUL
012	0	0CD	0011001101	2	0DD	0011011101	"	0CD	0011001101	2	0DD	0011011101	"
013	0	188	0110001000	W	1A8	0110101000	W	1E8	0111101000	ETB	1E8	0111101000	ETB
014	0	18E	0110001110	9	1AE	0110101110	Q	1EE	0111101110	DC1	1EE	0111101110	DC1
015	0	18C	0110001100	S	1AC	0110101100	S	1EC	0111101100	DC3	1EC	0111101100	DC3
016	0	19E	0110011110	a	1BE	0110111110	A	1FE	0111111110	SOH	1FE	0111111110	SOH
017	0	185	0110000101	Z	1A5	0110100101	Z	1E5	0111100101	SUB	1E5	0111100101	SUB
020	0	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL
021	0	0CB	0011001011	4	0DB	0011011011	$	0CB	0011001011	4	0DB	0011011011	$
022	0	0CC	0011001100	3	0DC	0011011100	#	0CC	0011001100	3	0DC	0011011100	#
023	0	18D	0110001101	r	1AD	0110101101	R	1ED	0111101101	DC2	1ED	0111101101	DC2
024	0	19A	0110011010	e	1BA	0110111010	E	1FA	0111111010	ENQ	1FA	0111111010	ENQ
025	0	198	0110011011	d	1B8	0110111011	D	1F8	0111111011	EOT	1F8	0111111011	EOT
026	0	187	0110000111	x	1A7	0110100111	X	1E7	0111100111	ETB	1E7	0111100111	ETB
027	0	19C	0110011100	c	1BC	0110111100	c	1FC	0111111100	ETX	1FC	0111111100	ETX
030	0	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH
031	0	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX
032	0	0CA	0011001010	5	0DA	0011011010	%	0CA	0011001010	5	0DA	0011011010	%
033	0	18B	0110001011	t	1AB	0110101011	T	1EB	0111101011	DC4	1EB	0111101011	DC4
034	0	199	0110011001	f	1B9	0110111001	F	1F9	0111111001	ACK	1F9	0111111001	ACK
035	0	198	0110011000	g	1B8	0110111000	G	1F8	0111111000	BEL	1F8	0111111000	BEL
036	0	189	0110001001	v	1A9	0110101001	V	1E9	0111101001	SYN	1E9	0111101001	SYN
037	0	19D	0110011101	b	1BD	0110111101	B	1FD	0111111101	STX	1FD	0111111101	STX
040	0	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX
041	0	0C8	0011001000	7	0D9	0011011001	¢	0C8	0011001000	7	0D9	0011011001	¢
042	0	0C9	0011001001	6	0D9	0011011001	¢	0C9	0011001001	6	0D9	0011011001	¢
043	0	186	0110000110	y	1A6	0110100110	Y	1E6	0111100110	EM	1E6	0111100110	EM
044	0	197	0110010111	h	1B7	0110110111	H	1F7	0111110111	BS	1F7	0111110111	BS
045	0	191	0110010001	n	1B1	0110110001	N	1F1	0111110001	SO	1F1	0111110001	SO
046	0	0C9	0011001001	6	0C3	0011000011	<	0C9	0011001001	6	0C3	0011000011	<
047	0	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP
050	0	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT
051	0	0C7	0011000111	8	0D5	0011010101	*	0C7	0011000111	8	0D5	0011010101	*
052	0	0C8	0011001000	7	0D8	0011011000	'	0C8	0011001000	7	0D8	0011011000	'
053	0	18A	0110001010	u	1AA	0110101010	u	1EA	0111101010	NAK	1EA	0111101010	NAK
054	0	195	0110010101	J	1B5	0110110101	J	1F5	0111110101	ENQ	1F5	0111110101	ENQ
055	0	194	0110010100	k	1B4	0110110100	K	1F4	0111110100	VT	1F4	0111110100	VT
056	0	192	0110010010	m	1B2	0110110010	M	1F2	0111110010	CR	1F2	0111110010	CR
057	0	0D3	0011010011	.	0C3	0011000011	<	0D3	0011010011		0C3	0011000011	<
060	0	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ
061	0	0C6	0011000110	9	0D7	0011010111	(	0C6	0011000110	9	0D7	0011010111	(
062	0	0C7	0011000111	8	0D7	0011010111	(	0C7	0011000111	8	0D7	0011010111	(
063	0	196	0110010110	i	1B6	0110110110	I	1F6	0111110110	HT	1F6	0111110110	HT
064	0	190	0110010000	o	1B0	0110110000	O	1F0	0111110000	SI	1F0	0111110000	SI
065	0	194	0110010100	K	1A4	0110100100	[	1F4	0111110100	VT	1E4	0111100100	ESC
066	0	193	0110010011	l	1B3	0110110011	L	1F3	0111110011	FF	1F3	0111110011	FF
067	0	192	0110010010	m	1A2	0110100010	]	1F2	0111110010	CR	1E2	0111100010	GS
070	0	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK
071	0	0CF	0011001111	Ø	0D6	0011010110	)	0CF	0011001111	Ø	0D6	0011010110	)
072	0	0C6	0011000110	9	0D6	0011010110	)	0C6	0011000110	9	0D6	0011010110	)
073	0	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL

CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
074	0	18F	0110001111	P	1AF	0110101111	P	1EF	0111101111	DLE	1EF	0111101111	DLE
075	0	0C4	0011000100	;	0C5	0011000101	:	0C4	0011000100	;	0C5	0011000101	:
076	0	193	0110010011	L	1A3	0110100011	\	1F3	0111110011	FF	1E3	0111100011	FS
077	0	0D1	0011010001	.	0C1	0011000001	>	0D1	0011010001	.	0C1	0011000001	>
080	0	0D2	0011010010	–	1A0	0110100000	–	0D2	0011010010	–	1A0	0110100000	–
081	0	191	0110010001	n	1A1	0110100001	^	1F1	0111110001	SI	1E1	0111100001	RS
082	0	18F	0110001111	P	1BF	0110111111	@	1EF	0111101111	DLE	1FF	0111111111	NUL
083	0	1A4	0110100100	[	1A2	0110100010	]	1E4	0111100100	ESC	1E2	0111100010	GS
084	0	0D8	0011011000	'	0DD	0011011101	"	0D8	0011011000	'	0DD	0011011101	"
085	0	0C4	0011000100	;	0D4	0011010100	+	0C4	0011000100	;	0D4	0011010100	+
086	0	0D0	0011010000	/	0C0	0011000000	?	0D0	0011010000	/	0C0	0011000000	?
087	0	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS
090	0	0C2	0011000010	=	0D4	0011010100	+	0C2	0011000010	=	0D4	0011010100	+
091	0	0C5	0011000101	:	0D5	0011010101	*	0C5	0011000101	:	0D5	0011010101	*
092	0	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT
093	0	1A3	0110100011	\	083	0010000011	!	1E3	0111100011	FS	1E3	0111100011	FS
094	0	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF
095	0	1A4	0110100100	[	084	0010000100	{	1E4	0111100100	ESC	1E4	0111100100	ESC
096	0	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR
097	0	1A2	0110100010	]	082	0010000010	}	1E2	0111100010	GS	1E2	0111100010	GS
100	0	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL
101	0	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT
102	0	0D2	0011010010	_	1A0	0110100000	_	1E0	0111100000	US	1E0	0111100000	US
103	0	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS
104	0	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF
105	0	1BF	0110111111	@	1A3	0110100011	\	1FF	0111111111	NUL	1FF	0111111111	NUL
106	0	1A1	0110100001	^	081	0010000001	~	1E1	0111100001	RS	1E1	0111100001	RS
107	0	1A0	0110100000	_	0C2	0011000010	=	1A0	0110100000	_	0C2	0011000010	=
110	0	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR
111	0	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT
112	0	0D2	0011010010	-	0C2	0011000010	=	0D2	0011010010	–	0C2	0011000010	=
113	0	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO
114	0	190	0110010000	o	1A0	0110100000	–	1F0	0111110000	SI	1E0	0111100000	US
115	0	1A4	0110100100	[	1A2	0110100010	]	1A4	0110100100	[	1A2	0110100010	]
116	0	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS
117	0	160	0101100000	US	160	0101100000	US	160	0101100000	US	160	0101100000	US
120	0	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI
121	0	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7
122	0	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT
123	0	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE
124	0	0CB	0011001011	4	0CB	0011001011	4	0CB	0011001011	4	0CB	0011001011	4
125	0	0D3	0011010011	,	0D3	0011010011	,	0DB	0011010011	,	0D3	0011010011	,
126	0	0CE	0011001110	I	0CE	0011001110	1	0CE	0011001110	I	0CE	0011001110	I
127	0	0CF	0011001111	Ø	0CF	0011001111	Ø	0CF	0011001111	Ø	0CF	0011001111	0
130	0	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1
131	0	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9
132	0	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8
133	0	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5
134	0	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6
135	0	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2
136	0	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3
137	0	0D1	0011010001		0D1	0011010001		0D1	0011010001		0D1	0011010001	

OPTIONS ARE: Error Flag — Programmed
X15 — Discrete output, normally low
KBINH — Set by high on pin 12 or error flag. Function keys not inhibited by KBINH
Error Flag — Reset by releasing error-causing key
Shift Lock — Operational. SLI normally low
Alpha Lock — Inhibited. ALI normally low, set by OP code XX101
D10 — Discrete output, normally low
Key Type — Normally open

NOTE: Bit 9 — Programmed to allow alpha lock implementation using external logic
Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes.
Bits 1-7 — "Inverted" ASCII data bits

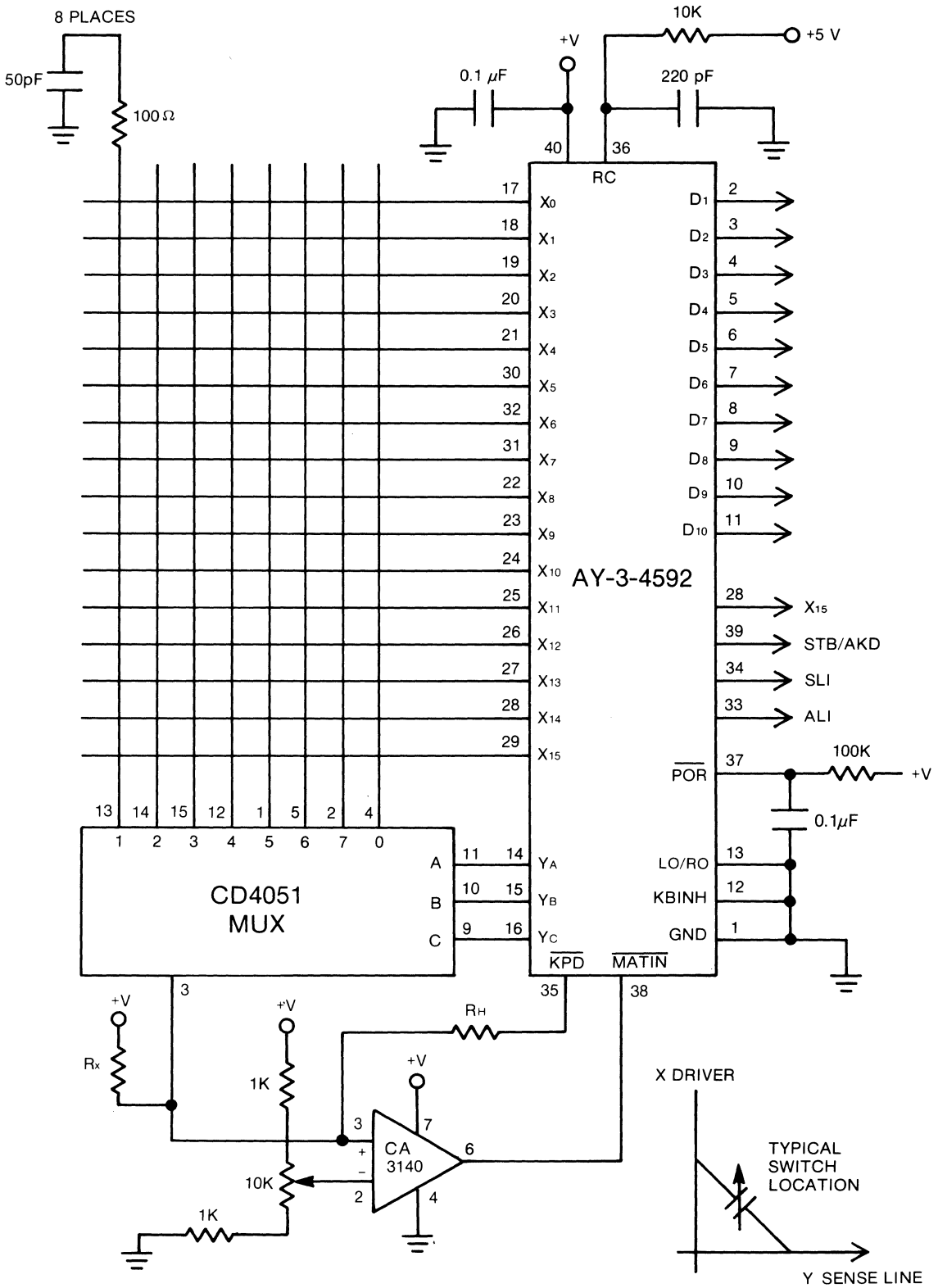


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

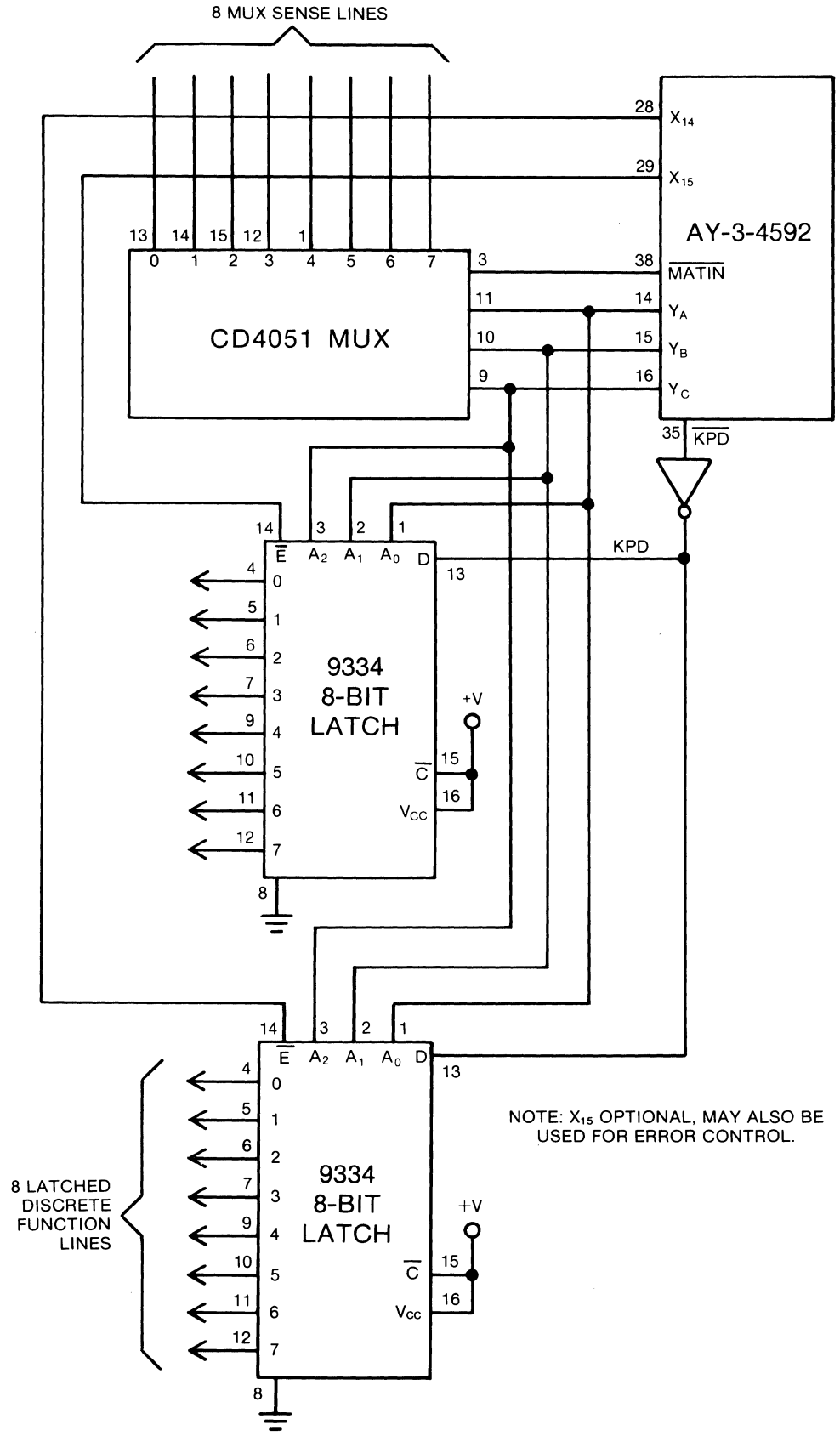


Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS

Character Generator

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CHARACTER GENERATOR	2,560 bits organized as 64 - 5 x 8 characters	RO-3-2513	3-44

Character Generator

FEATURES

- 64 x 8 x 5 Organization—ideal for systems requiring a row scan 5 x 7 dot matrix character generator
- Single +5 Volt Supply
- TTL Compatible — all inputs and outputs
- Static Operation — no clocks required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — under the control of an 'Output Inhibit' input to simplify memory expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programming Available
- Zener Protected Inputs
- Glass Passivation Protection

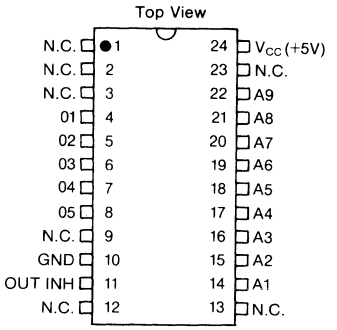
DESCRIPTION

The General Instrument RO-3-2513 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in General Instrument's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5 x 7 dot matrix format.

The RO-3-2513 is available pre-programmed with ASCII encoded 5 x 7 characters (General Instrument's part no. RO-3-2513/CGR-001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140. The RO-3-2513 is also available preprogrammed with lower case ASCII encoded 5 x 7 characters (General Instrument's part no. RO-3-2513/CGR-005), a direct replacement for the Signetics 2513/CM3021.

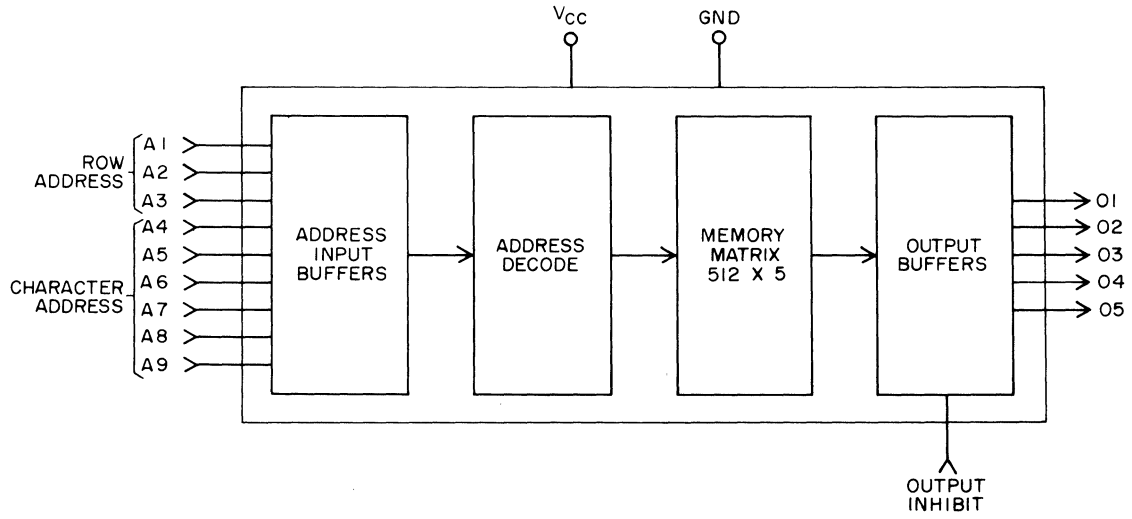
PIN CONFIGURATION

24 LEAD DUAL IN LINE



A separate publication, "RO-3-2513 Custom Coding Information," available from General Instrument's Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2513 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

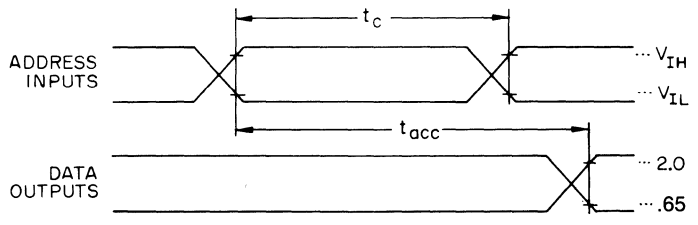
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF.

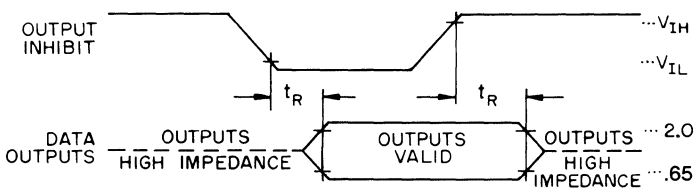
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	33	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-001 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

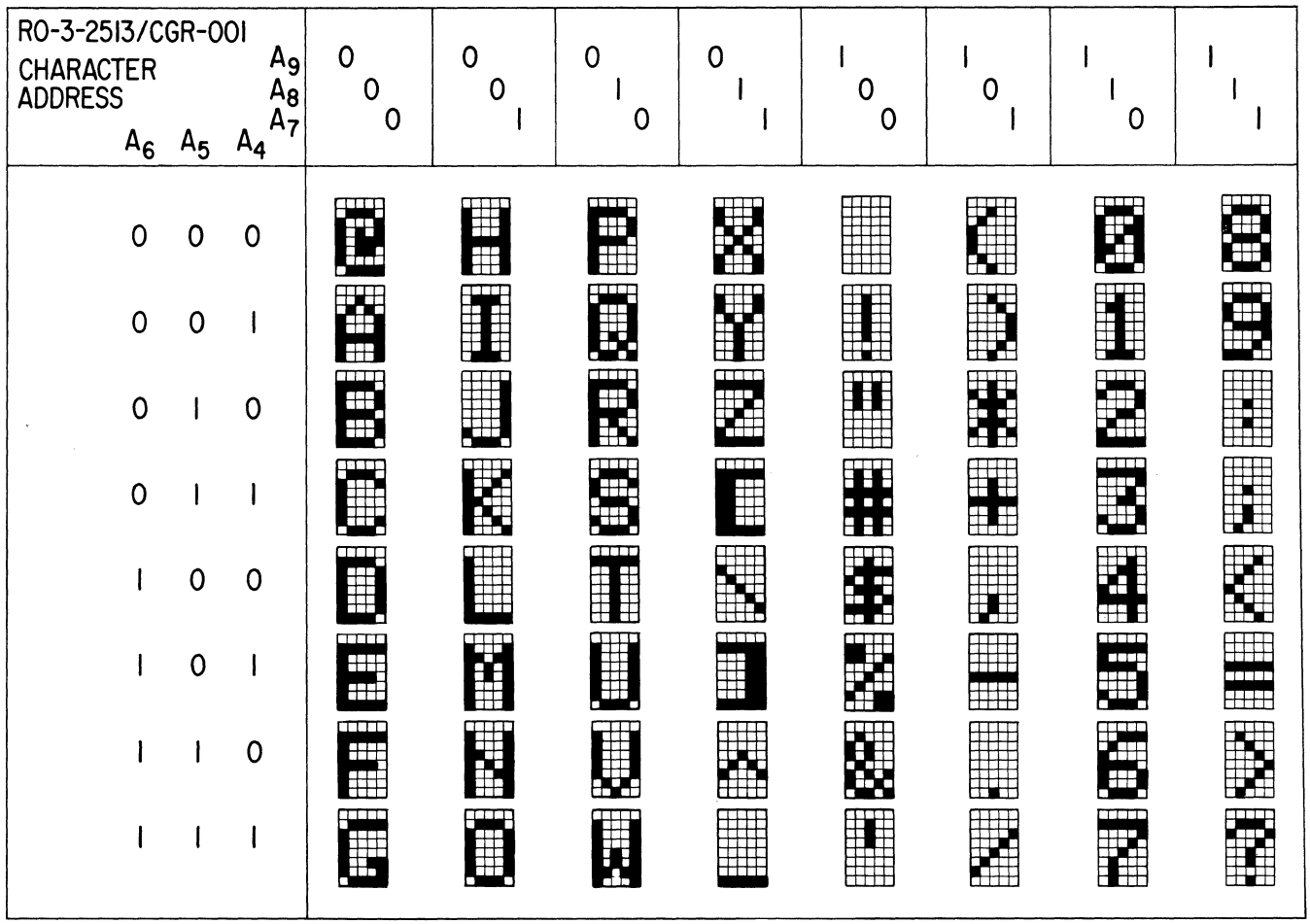
RO-3-2513/CGR-001 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII upper case "S" Character	0	1	0	0	1	1

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0



RO-3-2513-005 STANDARD PATTERN CHARACTER FORMAT (Lower Case ASCII)

The RO-3-2513/CGR-005 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

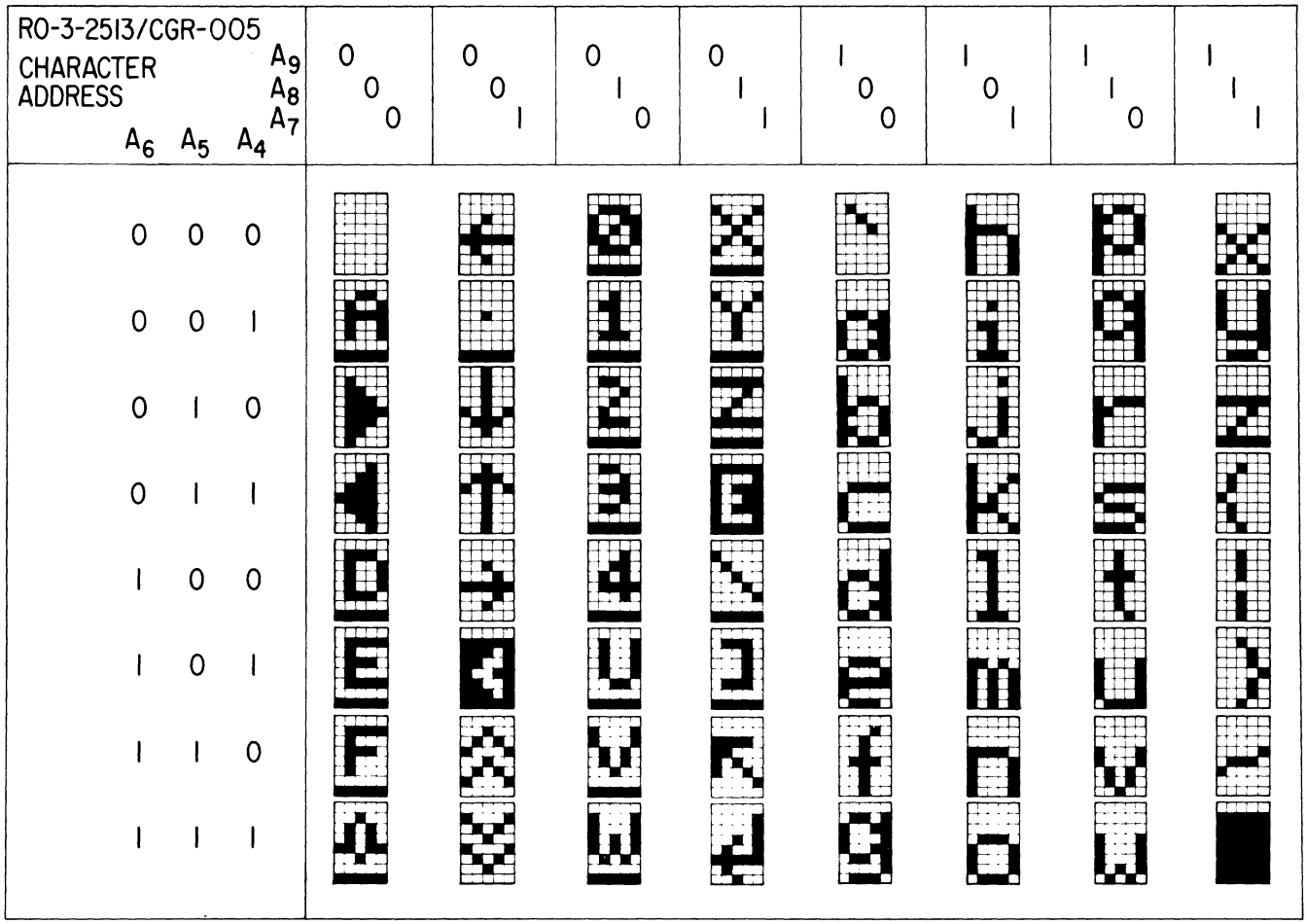
RO-3-2513/CGR-005 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII lower case 's' Character	1	1	0	0	1	1

ROW ADDRESS

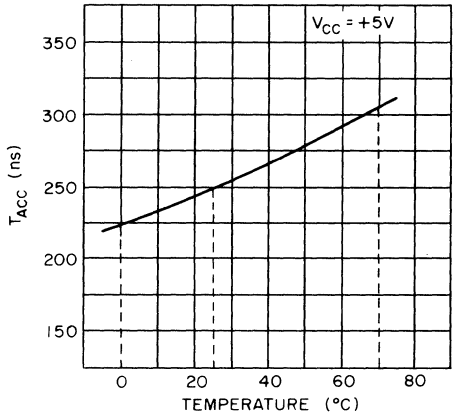
A3	A2	A1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

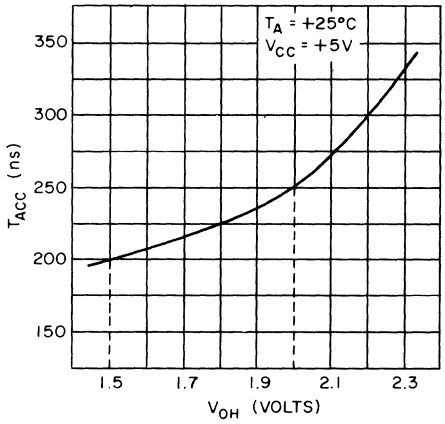
05	04	03	02	01
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	1	1	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	1	1	1	0



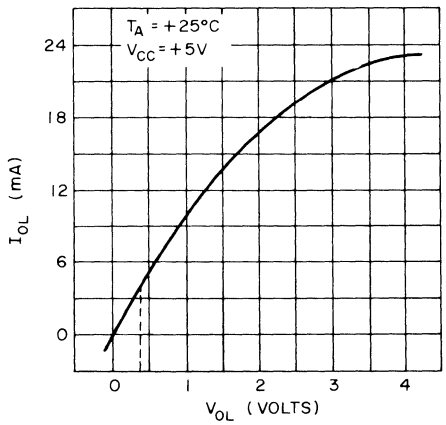
TYPICAL CHARACTERISTIC CURVES



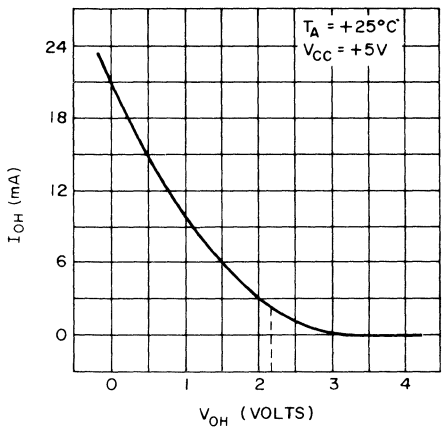
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

NOTES

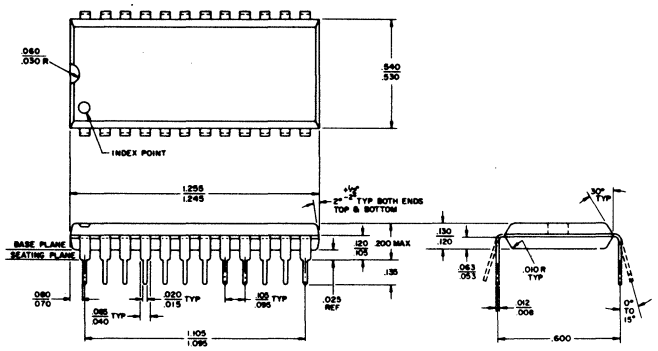
NOTES

NOTES

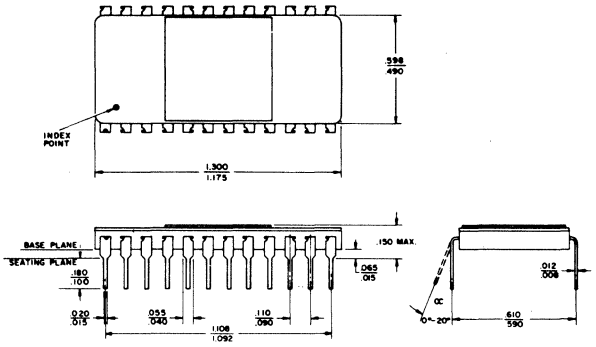
ROM

PACKAGE OUTLINES (All dimensions in inches)

24 LEAD DUAL IN LINE

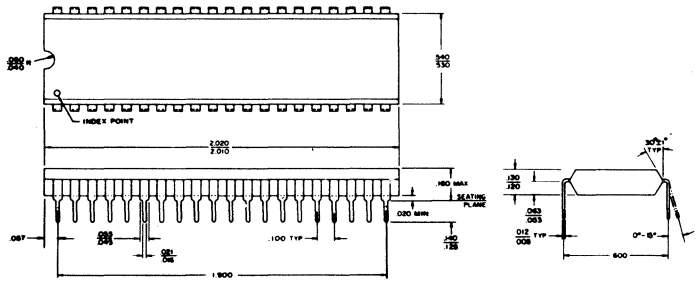


PLASTIC

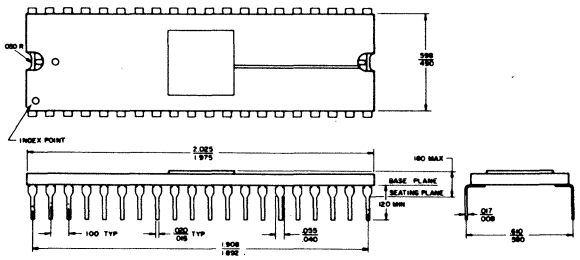


CERAMIC

40 LEAD DUAL IN LINE



PLASTIC



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